SHARC® Processor

Preliminary Technical Data

ADSP-21369

SUMMARY

High performance 32-bit/40-bit floating point processor optimized for high performance audio processing

Single-Instruction Multiple-Data (SIMD) computational architecture

On-chip memory—2M bit of on-chip SRAM and 6M bit of on-chip mask programmable ROM

Code compatible with all other members of the SHARC family

The ADSP-21369 is available with a 400 MHz core instruction rate with unique audio centric peripherals such as the Digital Audio Interface, S/PDIF transceiver, serial ports, 8-channel asynchronous sample rate converter, precision clock generators and more. For complete ordering information, see Ordering Guide on Page 52

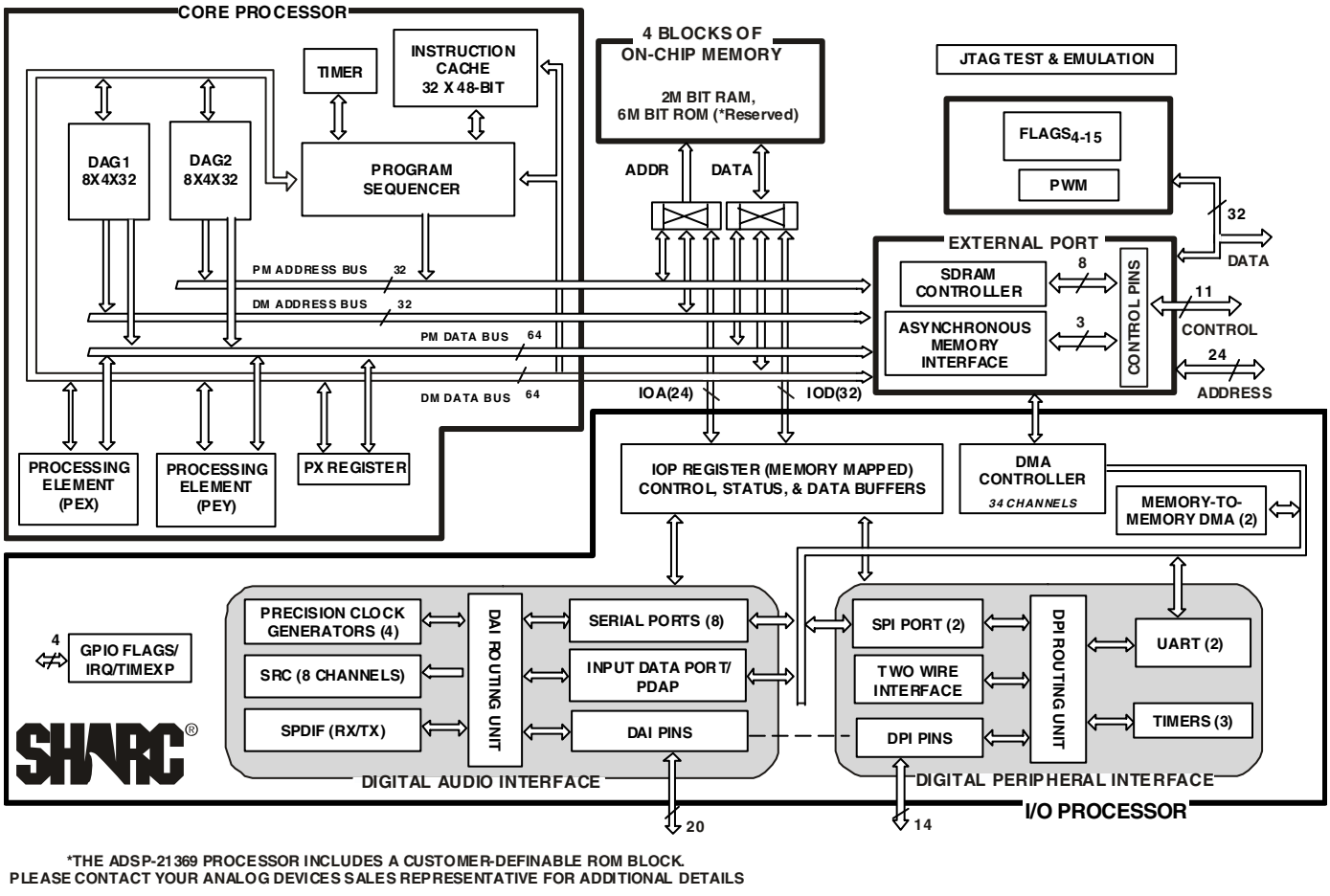

Figure 1. Functional Block Diagram

Rev. PrB

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 U.S.A.
Tel:781.329.4700 **www.analog.com**
Fax:781.326.8703

KEY FEATURES – PROCESSOR CORE

- At 400 MHz (2.5 ns) core instruction rate, the ADSP-21369 performs 2.4 GFLOPS/800 MMACS
- 2M bit on-chip, SRAM (0.75M Bit in blocks 0 and 1, and 250K bit in blocks 2 and 3) for simultaneous access by the core processor and DMA
- 6M bit on-chip, mask-programmable, ROM (3M bit in block 0 and 3M bit in block 1)
- Dual data address generators (DAGs) with modulo and bit-reverse addressing
- Zero-overhead looping with single-cycle loop setup, providing efficient program sequencing
- Single Instruction Multiple Data (SIMD) architecture provides:
  - Two computational processing elements
  - Concurrent execution
  - Code compatibility with other SHARC family members at the assembly level
  - Parallelism in buses and computational units allows: Single cycle executions (with or without SIMD) of a multiply operation, an ALU operation, a dual memory read or write, and an instruction fetch
- Transfers between memory and core at a sustained 6.4G bytes/s bandwidth at 400 MHz core instruction rate

INPUT/OUTPUT FEATURES

- DMA controller supports:
  - 34 zero-overhead DMA channels for transfers between ADSP-21369 internal memory and a variety of peripherals
  - 32-bit DMA transfers at peripheral clock speed, in parallel with full-speed processor execution
- 32-Bit wide external port provides glueless connection to both synchronous (SDRAM) and asynchronous memory devices
  - Programmable wait state options: 2 to 31 SCLK cycles
  - Delay-line DMA engine maintains circular buffers in external memory with tap/offset based reads
  - SDRAM accesses at 166MHz and asynchronous accesses at 66MHz
  - 4 memory select lines allows multiple external memory devices
- Digital audio interface (DAI) includes eight serial ports, four precision clock generators, an input data port, an S/PDIF transceiver, an 8-channel asynchronous sample rate converter, and a signal routing unit
- Digital peripheral interface (DPI) includes, three timers, two UARTs, two SPI ports, and a two wire interface port
  - Outputs of PCG's C and D can be driven on to DPI pins
- Eight dual data line serial ports that operate at up to 50M bits/s on each data line — each has a clock, frame sync and two data lines that can be configured as either a receiver or transmitter pair
- TDM support for telecommunications interfaces including 128 TDM channel support for newer telephony interfaces such as H.100/H.110
- Up to 16 TDM stream support, each with 128 channels per frame
- Companding selection on a per channel basis in TDM mode
- Input data port, configurable as eight channels of serial data or seven channels of serial data and up to a 20-bit wide parallel data channel
- Signal routing unit provides configurable and flexible connections between all DAI/DPI components
- 2 Muxed Flag/$\overline{\text{IRQ}}$ lines
- 1 Muxed Flag/Timer expired line /$\overline{\text{MS}}$ pin
- 1 Muxed Flag/$\overline{\text{IRQ}}$ /$\overline{\text{MS}}$ pin

DEDICATED AUDIO COMPONENTS

- S/PDIF Compatible Digital Audio receiver/transmitter supports EIAJ CP-340 (CP-1201), IEC-958, AES/EBU standards
  - Left-justified, I^2S or right-justified serial data input with 16, 18, 20 or 24-bit word widths (transmitter)
- Four independent Asynchronous Sample Rate Converters (SRC). Each converter has separate serial input and output ports, a deemphasis filter providing up to -128dB SNR performance, stereo sample rate converter (SRC) and supports left-justified, I^2S, TDM and right-justified modes and 24, 20, 18 and 16 audio data word lengths.
- Pulse Width Modulation provides:
  - 16 PWM outputs configured as four groups of four outputs supports center-aligned or edge-aligned PWM waveforms
- ROM Based Security features include:
  - JTAG access to memory permitted with a 64-bit key
  - Protected memory regions that can be assigned to limit access under program control to sensitive code
- PLL has a wide variety of software and hardware multiplier/divider ratios
- Dual voltage: 3.3 V I/O, 1.3 V core
- Available in 256-ball SBGA and 208-lead MQFP Packages (see Ordering Guide on Page 52)

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REVISION HISTORY

6/05–Data sheet changed from REV. PrA to REV. PrB

This revision corrects the pin assignments on the SBGA Ball Grid Array package. Pin V13 is now correctly identified as IOVDD, and pin V14 is GND. See Table 43 on page 48.

GENERAL DESCRIPTION

The ADSP-21369 SHARC processor is a members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. The ADSP-21369 is source code compatible with the ADSP-2126x, and ADSP-2116x, DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (Single-Instruction, Single-Data) mode. The ADSP-21369 is a 32-bit/40-bit floating point processors optimized for high performance automotive audio applications with its large on-chip SRAM, and mask-programmable ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative Digital Audio Interface (DAI).

As shown in the functional block diagram on Page 1, the ADSP-21369 uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the ADSP-21369 processor achieves an instruction cycle time of 2.5 ns at 400 MHz. With its SIMD computational hardware, the ADSP-21369 can perform 2.4 GFLOPS running at 400 MHz.

Table 1 shows performance benchmarks for the ADSP-21369.

Table 1. ADSP-21369 Benchmarks (at 400 MHz)

Benchmark Algorithm	Speed (at 400 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	23.25 µs
FIR Filter (per tap)[1]	1.25 ns
IIR Filter (per biquad)[1]	5.0 ns
Matrix Multiply (pipelined)	
[3x3] × [3x1]	11.25 ns
[4x4] × [4x1]	20.0 ns
Divide (y/x)	8.75 ns
Inverse Square Root	13.5 ns

[1] Assumes two files in multichannel SIMD mode

The ADSP-21369 continues SHARC's industry leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features.

The block diagram of the ADSP-21369 on Page 1, illustrates the following architectural features:

- Two processing elements, each of which comprises an ALU, Multiplier, Shifter and Data Register File
- Data Address Generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- Three Programmable Interval Timers with PWM Generation, PWM Capture/Pulse width Measurement, and External Event Counter Capabilities
- On-Chip SRAM (2M bit)
- On-Chip mask-programmable ROM (6M bit)
- JTAG test access port

The block diagram of the ADSP-21369 on Page 1 also illustrates the following architectural features:

- DMA controller
- Eight full duplex serial ports
- Digital audio interface that includes four precision clock generators (PCG), an input data port (IDP), an S/PDIF receiver/transmitter, eight channels asynchronous sample rate converters, eight serial ports, eight serial interfaces, a 16-bit parallel input port (PDAP), a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes three timers, an I^2C interface, two UARTs, two serial peripheral interfaces (SPI), and a flexible signal routing unit (DPI SRU).

ADSP-21369 FAMILY CORE ARCHITECTURE

The ADSP-21369 is code compatible at the assembly level with the ADSP-2126x, ADSP-21160 and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-21369 shares architectural features with the ADSP-2126x and ADSP-2116x SIMD SHARC processors, as detailed in the following sections.

SIMD Computational Engine

The ADSP-21369 contains two computational processing elements that operate as a Single-Instruction Multiple-Data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing ele-

ments. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-2136x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0-R15 and in PEY as S0-S15.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-21369 features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1 on page 1). With the ADSP-21369's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-21369 includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full-speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators With Zero-Overhead Hardware Circular Buffer Support

The ADSP-21369's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-21369 contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21369 can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

ADSP-21369 MEMORY

The ADSP-21369 adds the following architectural features to the SIMD SHARC family core.

On-Chip Memory

The ADSP-21369 contains two megabits of internal RAM and six megabits of internal mask-programmable ROM. Each block can be configured for different combinations of code and data storage (see Table 2). Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The ADSP-21369 memory architecture, in combination with its separate on-chip buses, allow two data transfers from the core and one from the I/O processor, in a single cycle.

The ADSP-21369's, SRAM can be configured as a maximum of 64K words of 32-bit data, 128K words of 16-bit data, 42K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to two megabits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

EXTERNAL MEMORY

The External Port on the ADSP-21369 SHARC provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The 32-bit wide bus may be used to interface to synchronous and/or asynchronous memory devices through the use of it's separate internal memory controllers: the first is an SDRAM controller for connection of industry-standard synchronous DRAM devices and DIMMs (Dual Inline Memory Module), while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types. Non SDRAM external memory address space is shown in Table 3.

SDRAM Controller

The SDRAM controller provides an interface to up to four separate banks of industry-standard SDRAM devices or DIMMs, at speeds up to f_{SCLK}. Fully compliant with the SDRAM standard, each bank can has it's own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 16M bytes and 128M bytes of memory. SDRAM external memory address space is shown in Table 4.

The controller maintains all of the banks as a contiguous address space so that the processor sees this as a single address space, even if different size devices are used in the different banks.

Table 2. ADSP-21369 Internal Memory Space [1]

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 bits)	**Extended Precision Normal or Instruction Word (48 bits)**	**Normal Word (32 bits)**	**Short Word (16 bits)**
BLOCK 0 ROM (Reserved) 0x0004 0000–0x0004 BFFF	BLOCK 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	BLOCK 0 ROM (Reserved) 0x0008 0000–0x0009 7FFF	BLOCK 0 ROM (Reserved) 0x0010 0000–0x0012 FFFF
Reserved 0x0004 F000–0x0004 FFFF	Reserved 0x0009 4000–0x0009 FFFF	Reserved 0x0009 E0000–0x0009 FFFF	Reserved 0x0013 C000–0x0013 FFFF
BLOCK 0 RAM 0x0004 C000–0x0004 EFFF	BLOCK 0 RAM 0x0009 0000–0x0009 3FFF	BLOCK 0 RAM 0x0009 8000–0x0009 DFFF	BLOCK 0 RAM 0x0013 0000–0x0013 BFFF
BLOCK 1 ROM (Reserved) 0x0005 0000–0x0005 BFFF	BLOCK 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	BLOCK 1 ROM (Reserved) 0x000A 0000–0x000B 7FFF	BLOCK 1 ROM (Reserved) 0x0014 0000–0x0016 FFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B 4000–0x000B FFFF	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
BLOCK 1 RAM 0x0005 C000–0x0005 EFFF	BLOCK 1 RAM 0x000B 0000–0x000B 3FFF	BLOCK 1 RAM 0x000B 8000–0x000B DFFF	BLOCK 1 RAM 0x0017 0000–0x0017 BFFF
BLOCK 2 RAM 0x0006 0000–0x0006 0FFF	BLOCK 2 RAM 0x000C 0000–0x000C 1554	BLOCK 2 RAM 0x000C 0000–0x000C 1FFF	BLOCK 2 RAM 0x0018 0000–0x0018 3FFF
Reserved 0x0006 1000–0x0006 FFFF	Reserved 0x000C 1555–0x000D FFFF	Reserved 0x000C 2000–0x000D FFFF	Reserved 0x0018 4000–0x001B FFFF
BLOCK 3 RAM 0x0007 0000–0x0007 0FFF	BLOCK 3 RAM 0x000E 0000–0x000E 1554	BLOCK 3 RAM 0x000E 0000–0x000E 1FFF	BLOCK 3 RAM 0x001C 0000–0x001C 3FFF
Reserved 0x0007 1000–0x0007 FFFF	Reserved 0x000E 1555–0x000F FFFF	Reserved 0x000E 2000–0x000F FFFF	Reserved 0x001C 4000–0x001F FFFF

[1] The ADSP-21369 processor includes a customer-definable ROM block. Please contact your Analog Devices sales representative for additional details.

Table 3. External Memory for Non SDRAM Addresses

Bank	Size in words	Address Range
Bank 0	12M	0x0020 0000 – 0x00FF FFFF
Bank 1	16M	0x0400 0000 – 0x04FF FFFF
Bank 2	16M	0x0800 0000 – 0x08FF FFFF
Bank 3	16M	0x0C00 0000 – 0x0CFF FFFF

Table 4. External Memory for SDRAM Addresses

Bank	Size in words	Address Range
Bank 0	60M	0x0020 0000 – 0x03FF FFFF
Bank 1	64M	0x0400 0000 – 0x07FF FFFF
Bank 2	64M	0x0800 0000 – 0x0BFF FFFF
Bank 3	64M	0x0C00 0000 – 0x0FFF FFFF

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. The memory banks can be configured as either 32 bits wide for maximum performance and bandwidth or 16 bits wide for minimum device count and lower system cost.

The SDRAM controller address, data, clock, and command pins can drive loads up to 30 pF. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Asynchronous Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, ROM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank0 occupies a 14.7M word window and banks 1, 2, and 3 occupy a 16M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic. The banks can also be configured as 8-bit, 16-bit, or 32-bit wide buses for ease of interfacing to a range of memories and I/O devices tailored either to high performance or to low cost and power.

The asynchronous memory controller is capable of a maximum throughput of 267M bytes/sec using a 66MHz external bus speed. Other features include 8 to 32-bit and 16 to 32-bit packing and unpacking, booting from Bank Select 1, and support for delay line DMA.

ADSP-21369 INPUT/OUTPUT FEATURES

The ADSP-21369 I/O processor provides 34 channels of DMA, as well as an extensive set of peripherals. These include a 20 pin Digital Audio Interface which controls:

- Eight serial ports
- S/PDIF Receiver/Transmitter
- Four precision clock generators
- Four stereo sample rate converters
- Internal data port/parallel data acquisition port

The ADSP-21369 processor also contains a 14 pin Digital Peripheral Interface which controls:

- Three general-purpose timers
- Two Serial Peripheral Interfaces
- Two universal asynchronous receiver/transmitters (UARTs)
- A two wire interface/I^2C

DMA Controller

The ADSP-21369's on-chip DMA controller allows data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-21369's internal memory and its serial ports, the SPI-compatible (Serial Peripheral Interface) ports, the IDP (Input Data Port), the Parallel Data Acquisition Port (PDAP) or the UART. Thirty-four channels of DMA are available on the ADSP-21369—sixteen via the serial ports, eight via the Input Data Port, four for the UARTs, two for the SPI interface, two for the external port, and two for memory-to-memory transfers. Programs can be downloaded to the ADSP-21369 using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

Delay Line DMA

The ADSP-21369 processor provides Delay Line DMA functionality. This allows processor reads and writes to external Delay Line Buffers (and hence to external memory) with limited core interaction.

Digital Audio Interface (DAI)

The Digital Audio Interface (DAI) provides the ability to connect various peripherals to any of the DSPs DAI pins (DAI_P20–1).

Programs make these connections using the Signal Routing Unit (SRU, shown in Figure 1.

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with non configurable signal paths.

The DAI also includes eight serial ports, an S/PDIF receiver/transmitter, four precision clock generators (PCG), eight channels of synchronous sample rate converters, and an input data port (IDP). The IDP provides an additional input path to the ADSP-21369 core, configurable as either eight channels of I^2S serial data or as seven channels plus a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the ADSP-21369's serial ports.

For complete information on using the DAI, see the *ADSP-2136x SHARC Processor Hardware Reference for the ADSP-21367/8/9 Processors*.

Serial Ports

The ADSP-21369 features eight synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog devices AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports are enabled via 16 programmable and simultaneous receive or transmit pins that support up to 32 transmit or 32 receive channels of audio data when all eight SPORTS are enabled, or eight full duplex TDM streams of 128 channels per frame.

The serial ports operate at a maximum data rate of 50M bits/s. Serial port data can be automatically transferred to and from on-chip memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode with support for Packed I^2S mode
- I^2S mode
- Packed I^2S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample pair and I^2S protocols (I^2S is an industry standard interface commonly used by audio codecs, ADCs and DACs such as the

Analog Devices AD183x family), with two data pins, allowing four left-justified sample pair or I²S channels (using two stereo devices) per serial port, with a maximum of up to 32 I²S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I²S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

The serial ports also contain frame sync error detection logic where the serial ports detect frame syncs that arrive early (for example frame syncs that arrive while the transmission/reception of the previous word is occurring). All the serial ports also share one dedicated error interrupt.

S/PDIF Compatible Digital Audio Receiver/Transmitter and Synchronous/Asynchronous Sample Rate Converter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left justified, I²S or right justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the Signal Routing Unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), or the sample rate converters (SRC) and are controlled by the SRU control registers.

The sample rate converter (SRC) contains four SRC blocks and is the same core as that used in the AD1896 192 kHz Stereo Asynchronous Sample Rate Converter and provides up to 128dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC is used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Digital Peripheral Interface (DPI)

The Digital Peripheral Interface provides connections to two serial peripheral interface ports (SPI), two universal asynchronous receiver-transmitters (UARTs), a Two Wire Interface (TWI), 12 Flags, and three general-purpose timers.

Serial Peripheral (Compatible) Interface

The ADSP-21369 SHARC processor contains two Serial Peripheral Interface ports (SPIs). The SPI is an industry standard synchronous serial link, enabling the ADSP-21369 SPI compatible port to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI compatible devices, either acting as a master or slave device. The ADSP-21369 SPI compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The ADSP-21369 SPI compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The ADSP-21369 processor provides a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (Programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (Direct Memory Access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/ 1,048,576) to (f_{SCLK}/16) bits per second.
- Supporting data formats from 7 to12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

Where the 16-bit UART_Divisor comes from the DLH register (most significant 8 bits) and DLL register (least significant 8 bits).

In conjunction with the general-purpose timer functions, autobaud detection is supported.

Timers

The ADSP-21369 has a total of four timers: a core timer that can generate periodic software interrupts and three general purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse Waveform Generation mode
- Pulse Width Count /Capture mode
- External Event Watchdog mode

The core timer can be configured to use FLAG3 as a Timer Expired signal, and each general purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register,

a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables all three general purpose timers independently.

Two Wire Interface Port (TWI)

The TWI is a bi-directional 2-wire, serial bus used to move 8-bit data while maintaining compliance with the I2C bus protocol. The TWI Master incorporates the following features:

- Simultaneous Master and Slave operation on multiple device systems with support for multi master data arbitration
- Digital filtering and timed event processing
- 7 and 10 bit addressing
- 100K bits/s and 400K bits/s data rates
- Low interrupt rate

Pulse Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the mid-point of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the mid-point of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

ROM Based Security

The ADSP-21369 has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the processor does not boot-load any external code, executing exclusively from internal SRAM/ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or Test Access Port will be assigned to each customer. The device will ignore a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the ADSP-21369 boots at system power-up from an 8-bit EPROM via the external port, an SPI master, an SPI slave or an internal boot. Booting is determined by the Boot Configuration (BOOTCFG1–0) pins (see Table 7 on page 15). Selection of the boot source is controlled via the SPI as either a master or slave device, or it can immediately begin executing from ROM.

Power Supplies

The ADSP-21369 has separate power supply connections for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (A_{VDD}/A_{VSS}) power supplies. The internal and analog supplies must meet the 1.3V requirement. The external supply must meet the 3.3V requirement. All external supply pins must be connected to the same power supply.

Note that the analog supply pin (A_{VDD}) powers the ADSP-21369's internal clock generator PLL. To produce a stable clock, it is recommended that PCB designs use an external filter circuit for the A_{VDD} pin. Place the filter components as close as possible to the A_{VDD}/A_{VSS} pins. For an example circuit, see Figure 2. (A recommended ferrite chip is the muRata BLM18AG102SN1D). To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DDINT} and GND. Use wide traces to connect the bypass capacitors to the analog power (A_{VDD}) and ground (A_{VSS}) pins. Note that the A_{VDD} and A_{VSS} pins specified in Figure 2 are inputs to the processor and not the analog ground plane on the board—the A_{VSS} pin should connect directly to digital ground (GND) at the chip.

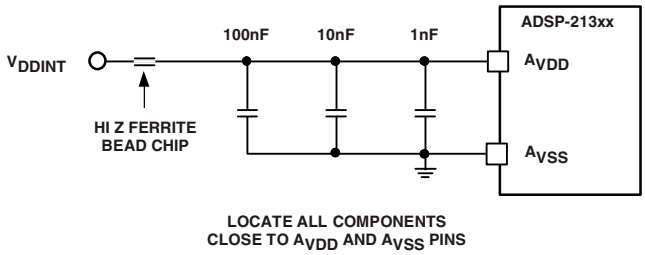


Figure 2. Analog Power (A_{VDD}) Filter Circuit

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-21369 processor to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate "Emulator Hardware User's Guide".

DEVELOPMENT TOOLS

The ADSP-21369 is supported with a complete set of CROSSCORE® software and hardware development tools, including Analog Devices emulators and VisualDSP++® development environment. The same emulator hardware that supports other SHARC processors also fully emulates the ADSP-21369.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler (which is based on an algebraic syntax), an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ runtime library that includes DSP and mathematical functions. A key point for these tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to DSP assembly. The SHARC has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to non intrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ IDDE lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all of the SHARC development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permits programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the tool's command line switches

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning, when developing new application code. The VDK features include Threads, Critical and Unscheduled regions, Semaphores, Events, and Device flags. The VDK also supports Priority-based, Preemptive, Cooperative, and Time-Sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK based objects, and visualizing the system state, when debugging an application that uses the VDK.

VisualDSP++ Component Software Engineering (VCSE) is Analog Devices' technology for creating, using, and reusing software components (independent modules of substantial functionality) to quickly and reliably assemble software applications. Download components from the Web and drop them into the application. Publish component archives from within VisualDSP++. VCSE supports component implementation in C/C++ or assembly language.

Use the Expert Linker to visually manipulate the placement of code and data on the embedded system. View memory utilization in a color-coded graphical form, easily move code and data to different areas of the processor or external memory with the drag of the mouse, examine run time stack and heap usage. The Expert Linker is fully compatible with the existing Linker Definition File (LDF), allowing the developer to move between the graphical and textual environments.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC processor PC plug-in cards. Third party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

Designing an Emulator-Compatible DSP Board (Target)

The Analog Devices family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on each JTAG DSP. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

Evaluation Kit

Analog Devices offers a range of EZ-KIT Lite evaluation platforms to use as a cost effective method to learn more about developing or prototyping applications with Analog Devices processors, platforms, and software tools. Each EZ-KIT Lite includes an evaluation board along with an evaluation suite of the VisualDSP++ development and debugging environment with the C/C++ compiler, assembler, and linker. Also included are sample application programs, power supply, and a USB cable. All evaluation versions of the software tools are limited for use only with the EZ-KIT Lite product.

The USB controller on the EZ-KIT Lite board connects the board to the USB port of the user's PC, enabling the VisualDSP++ evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also allows in-circuit programming of the on-board Flash device to store user-specific boot code, enabling the board to run as a standalone unit without being connected to the PC.

With a full version of VisualDSP++ installed (sold separately), engineers can develop software for the EZ-KIT Lite or any custom defined system. Connecting one of Analog Devices JTAG emulators to the EZ-KIT Lite board enables high-speed, nonintrusive emulation.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21369 architecture and functionality. For detailed information on the ADSP-2136x Family core architecture and instruction set, refer to the *ADSP-2136x SHARC Processor Hardware Reference for the ADSP-21367/8/9 Processors* and the *ADSP-2136x SHARC Processor Programming Reference*.

PIN FUNCTION DESCRIPTIONS

The following symbols appear in the Type column of Table 5: A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, and T = Three-State, (pd) = pull-down resistor, (pu) = pull-up resistor.

Table 5. Pin List

Name	Type	State During and After Reset	Description
$ADDR_{23-0}$	I/O with programmable pu[1]	Three state with pull-up enabled, driven low	**External Address.** The ADSP-21369 outputs addresses for external memory and peripherals on these pins.
$DATA_{31-0}$	I/O with programmable pu	Three-state with pull-up enabled	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O), the PDAP (I), FLAGS (I/O), and PWM (O). After reset, all DATA pins will be in EMIF mode and FLAG(0-3) pins will be in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP Channel 0 scans the $DATA_{31-8}$ pins for parallel input data.
DAI _P_{20-1}	I/O with programmable pu[2]	Three-state with programmable pull-up	**Digital Audio Interface Pins**. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audio centric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins. The DAI SRU provides the connection from the serial ports (8), the SRC module, the PWM module, the S/PDIF module, input data ports (2), and the precision clock generators (4), to the DAI_P20–1 pins.
DPI _P_{14-1}	I/O with programmable pu[2]	Three-state with programmable pull-up	**Digital Peripheral Interface.** These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins. The DPI SRU provides the connection from the timers (3), SPIs (2), UARTs (2), flags (12) I^2C (1), and general-purpose I/O (9) to the DPI_P14–1 pins. The I^2C output is an open-drain output—so the pins used for I^2C data and clock should be connected to logic level 0.
ACK	Input with programmable pu[1]		**Memory Acknowledge.** External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{RD}$	Output with programmable pu[1]	Pull-up, driven high	**External Port Read Enable.** $\overline{RD}$ is asserted whenever the ADSP-21369 reads a word from external memory. $\overline{RD}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{WR}$	Output with pu[1]	Pull-up, driven high	**External Port Write Enable.** $\overline{WR}$ is asserted when the ADSP-21369 writes a word to external memory. $\overline{WR}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{SDRAS}$	Output with pu[1]	Pull-up, driven high	**SDRAM Row Address Strobe.** Connect to SDRAM's RAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{SDCAS}$	Output with pu[1]	Pull-up, driven high	**SDRAM Column Address Select.** Connect to SDRAM's CAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{SDWE}$	Output with pu[1]	Pull-up, driven high	**SDRAM Write Enable.** Connect to SDRAM's WE or W buffer pin.

Table 5. Pin List

Name	Type	State During and After Reset	Description
SDCKE	Output with pu[1]	Pull-up, driven high	**SDRAM Clock Enable.** Connect to SDRAM's CKE pin. Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	Output with pu[1]	Pull-up, driven high	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with a non-SDRAM accesses. This pin replaces the DSP's A10 pin only during SDRAM accesses.
SDCLK0	I/O		**SDRAM Clock Configure.**
$\overline{MS}_{0-1}$	I/O with programmable pu[1]		**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the MS3-0 lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true.
FLAG[0]/$\overline{IRQ0}$	I/O		**FLAG0/Interrupt Request0.**
FLAG[1]/$\overline{IRQ1}$	I/O		**FLAG1/Interrupt Request1.**
FLAG[2]/$\overline{IRQ2}$/$\overline{MS2}$	I/O with programmable[1] pu (for MS mode)		**FLAG2/Interrupt Request/Memory Select2.**
FLAG[3]/TIMEXP/$\overline{MS3}$	I/O with programmable[1] pull-up (for MS mode)		**FLAG3/Timer Expired/Memory Select3.**
TDI	Input with pu		**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 22.5 kΩ internal pull-up resistor.
TDO	Output		**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	Input with pu		**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 22.5 kΩ internal pull-up resistor.
TCK	Input		**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21369.
$\overline{TRST}$	Input with pu		**Test Reset (JTAG).** Resets the test state machine. $\overline{TRST}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21369. $\overline{TRST}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{EMU}$	Output with pu		**Emulation Status.** Must be connected to the ADSP-21369 Analog Devices DSP Tools product line of JTAG emulators target board connector only. $\overline{EMU}$ has a 22.5 kΩ internal pull-up resistor.
CLK_CFG_{1-0}	Input		**Core/CLKIN Ratio Control.** These pins set the start up clock frequency. See Table 8 for a description of the clock configuration modes. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset.
$BOOT\_CFG_{1-0}$	Input		**Boot Configuration Select.** These pins select the boot mode for the processor. The BOOTCFG pins must be valid before reset is asserted. See Table 7 for a description of the boot modes.

Table 5. Pin List

Name	Type	State During and After Reset	Description
$\overline{\text{RESET}}$	Input		**Processor Reset.** Resets the ADSP-21369 to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
XTAL	Output		**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.
CLKIN	Input		**Local Clock In.** Used in conjunction with XTAL. CLKIN is the ADSP-21369 clock input. It configures the ADSP-21369 to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the ADSP-21369 to use the external clock source such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency.
CLKOUT	Output		**Local Clock Out.** CLKOUT can also be configured as a reset out pin.The functionality can be switched between the PLL output clock and reset out by setting bit 12 of the PMCTREG register. The default is reset out.

[1] Pull-up is always enabled
[2] Pull-up can be enabled/disabled, value of pull-up cannot be programmed.

DATA MODES

The upper 32 data pins of the external memory interface are muxed (using bits in the SYSCTL register) to support the external memory interface data (input/output), the PDAP (input only), the FLAGS (input/output), and the PWM channels (output). Table 6 provides the pin settings.

Table 6. Function of Data Pins

DATA PIN MODE	DATA31–16	DATA15–8	DATA7–0
000	EPDATA32–0		
001	FLAGS/PWM15–0[1]	EPDATA15–0	
010	FLAGS/PWM15–0[1]	FLAGS15–8	EPDATA7–0
011	FLAGS/PWM15–0[1]	FLAGS15–0	
100	PDAP (DATA + CTRL)		EPDATA7–0
101	PDAP (DATA + CTRL)		FLAGS7–0
110	Reserved		
111	Three-state all pins		

[1] These signals can be FLAGS or PWM or a mix of both. However, they can be selected only in groups of four. Their function is determined by the control signals FLAGS/PWM_SEL. For more information, see the *ADSP-2136x SHARC Processor Hardware Reference for the ADSP-21367/8/9 Processors*.

BOOT MODES

Table 7. Boot Mode Selection

BOOTCFG1–0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	EPROM/FLASH Boot

CORE INSTRUCTION RATE TO CLKIN RATIO MODES

For details on processor timing, see Timing Specifications and Figure 3 on Page 18.

Table 8. Core Instruction Rate/ CLKIN Ratio Selection

CLKCFG1–0	Core to CLKIN Ratio
00	6:1
01	32:1
10	16:1

ADSP-21369 SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter[1]		K Grade		B Grade[2]		
		Min	Max	Min	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	1.235	1.365	1.235	1.365	V
A_{VDD}	Analog (PLL) Supply Voltage	1.235	1.365	1.235	1.365	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	V
V_{IH}[3]	High Level Input Voltage @ V_{DDEXT} = max	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	V
V_{IL}[3]	Low Level Input Voltage @ V_{DDEXT} = min	–0.5	+0.8	–0.5	+0.8	V
V_{IH_CLKIN}[4]	High Level Input Voltage @ V_{DDEXT} = max	1.74	V_{DDEXT} + 0.5	1.74	V_{DDEXT} + 0.5	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DDEXT} = min	–0.5	+1.19	–0.5	+1.19	V
T_{AMB}[5, 6]	Ambient Operating Temperature	0	+70	–40	+85	°C

[1] Specifications subject to change without notice.
[2] Pending package qualification.
[3] Applies to input and bidirectional pins: AD23–0, DATA31–0, FLAG3–0, DAI_Px, DPI_Px, $\overline{SPIDS}$, BOOTCFGx, CLKCFGx, $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.
[4] Applies to input pin CLKIN.
[5] See Thermal Characteristics on Page 46 for information on thermal specifications.
[6] See Engineer-to-Engineer Note (No. TBD) for further information.

ELECTRICAL CHARACTERISTICS

Parameter[1]		Test Conditions	Min	Max	Unit
V_{OH}[2]	High Level Output Voltage	@ V_{DDEXT} = min, I_{OH} = –1.0 mA[3]	2.4		V
V_{OL}[2]	Low Level Output Voltage	@ V_{DDEXT} = min, I_{OL} = 1.0 mA[3]		0.4	V
I_{IH}[4, 5]	High Level Input Current	@ V_{DDEXT} = max, V_{IN} = V_{DDEXT} max		10	µA
I_{IL}[4]	Low Level Input Current	@ V_{DDEXT} = max, V_{IN} = 0 V		10	µA
I_{ILPU}[5]	Low Level Input Current Pull-up	@ V_{DDEXT} = max, V_{IN} = 0 V		200	µA
I_{OZH}[6, 7]	Three-State Leakage Current	@ V_{DDEXT}= max, V_{IN} = V_{DDEXT} max		10	µA
I_{OZL}[6]	Three-State Leakage Current	@ V_{DDEXT} = max, V_{IN} = 0 V		10	µA
I_{OZLPU}[7]	Three-State Leakage Current Pull-up	@ V_{DDEXT} = max, V_{IN} = 0 V		200	µA
$I_{DD-INTYP}$[8, 9]	Supply Current (Internal)	t_{CCLK} = 5.0 ns, V_{DDINT} = 1.3		500	mA
AI_{DD}[10]	Supply Current (Analog)	A_{VDD} = max		10	mA
C_{IN}[11, 12]	Input Capacitance	f_{IN}=1 MHz, T_{CASE}=25°C, V_{IN}=1.3V		4.7	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: ADDR23-0, DATA31-0, $\overline{RD}$, $\overline{WR}$, ALE, FLAG3–0, DAI_Px, DPI_Px, $\overline{EMU}$, TDO, CLKOUT, XTAL.
[3] See Output Drive Currents on Page 46 for typical drive current capabilities.
[4] Applies to input pins: BOOTCFGx, CLKCFGx, TCK, $\overline{RESET}$, CLKIN.
[5] Applies to input pins with 22.5 kΩ internal pull-ups: $\overline{TRST}$, TMS, TDI.
[6] Applies to three-statable pins: FLAG3–0.
[7] Applies to three-statable pins with 22.5 kΩ pull-ups: DAI_Px, DPI_Px, $\overline{EMU}$.
[8] Typical internal current data reflects nominal operating conditions.
[9] See Engineer-to-Engineer Note (No. TBD) for further information.
[10] Characterized, but not tested.
[11] Applies to all signal pins.
[12] Guaranteed, but not tested.

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})[1]	–0.3 V to +1.5 V
Analog (PLL) Supply Voltage (A_{VDD})[1]	–0.3 V to +1.5 V
External (I/O) Supply Voltage (V_{DDEXT})[1]	–0.3 V to +4.6 V
Input Voltage –0.5 V to V_{DDEXT}[1]	+0.5 V
Output Voltage Swing –0.5 V to V_{DDEXT}[1]	+0.5 V
Load Capacitance[1]	200 pF
Storage Temperature Range[1]	–65°C to +150°C
Junction Temperature under Bias	125°C

[1] Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The data in this table is based on theta JA (θ_{JA}) established per JEDEC standards JESD51-2 and JESD51-6. See Engineer-to-Engineer note (EE-TBD) for further information. For information on package thermal specifications, see Thermal Characteristics on Page 46.

Max Ambient Temp[1]	208 LQFP	256 SBGA
70°C	TBD W	TBD W
85°C	TBD W	TBD W

[1] Power Dissipation greater than that listed above may cause permanent damage to the device. For more information, see Thermal Characteristics on page 46.

ESD SENSITIVITY

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21369 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

The ADSP-21369's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLKCFG1–0 pins (see Table 8 on page 15). To determine switching frequencies for the serial ports, divide down the internal clock, using the programmable divider control of each port (DIVx for the serial ports).

The ADSP-21369's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Figure 3 shows Core to CLKIN ratios of 6:1, 16:1 and 32:1 with external oscillator or crystal. Note that more ratios are possible and can be set through software using the power management control register (PMCTL). For more information, see the *ADSP-2136x SHARC Processor Programming Reference*.

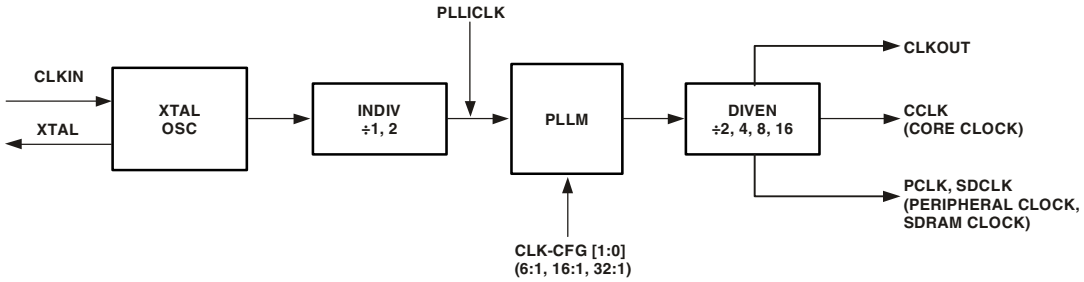


Figure 3. Core Clock and System Clock Relationship to CLKIN

Note the definitions of various clock periods shown in Table 10 which are a function of CLKIN and the appropriate ratio control shown in Table 9.

Table 9. ADSP-21369 CLKOUT and CCLK Clock Generation Operation

Timing Requirements	Description	Calculation
CLKIN	Input Clock	$1/t_{CK}$
CCLK	Core Clock	$1/t_{CCLK}$

Table 10. Clock Periods

Timing Requirements	Description[1]
t_{CK}	CLKIN Clock Period
t_{CCLK}	(Processor) Core Clock Period
t_{PCLK}	(Peripheral) Clock Period = 2 × t_{CCLK}
t_{SCLK}	Serial Port Clock Period = (t_{PCLK}) × SR
t_{SDCLK}	SDRAM Clock Period = (t_{CCLK}) × SDR
t_{SPICLK}	SPI Clock Period = (t_{PCLK}) × SPIR

[1] where:
SR = serial port-to-core clock ratio (wide range, determined by SPORT CLKDIV bits in DIVx register)
SPIR = SPI-to-Core Clock Ratio (wide range, determined by SPIBAUD register setting)
SPICLK = SPI Clock
SDR=SDRAM-to-Core Clock Ratio (Values determined by bits 20-18 of the PMCTL register)

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 38 on page 46 under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Power-Up Sequencing

The timing requirements for processor startup are given in Table 11.

Table 11. Power Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} on Before V_{DDEXT}	–50	200	ms
t_{CLKVDD} [1]	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10 [2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20 [3]		µs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096t_{CK} + 2\ t_{CCLK}$ [4, 5]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.3 and 3.3 volt rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's datasheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of 4 CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on t_{SRST} specification in Table 13. If setup time is not met, 1 additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

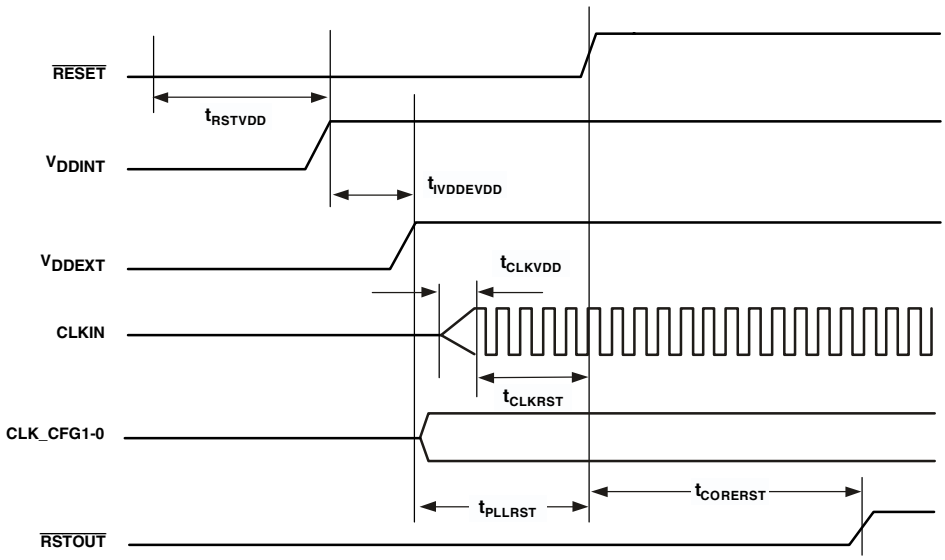


Figure 4. Power-Up Sequencing

Clock Input

Table 12. Clock Input

Parameter		400 MHz		Unit
		Min	Max	
Timing Requirements				
t_{CK}	CLKIN Period	15[1]	320[2]	ns
t_{CKL}	CLKIN Width Low	6[1]	150[2]	ns
t_{CKH}	CLKIN Width High	6[1]	150[2]	ns
t_{CKRF}	CLKIN Rise/Fall (0.4V–2.0V)		TBD	ns
t_{CCLK}[3]	CCLK Period	2.5[1]	10	ns

[1] Applies only for CLKCFG1–0 = 00 and default values for PLL control bits in PMCTL.
[2] Applies only for CLKCFG1–0 = 01 and default values for PLL control bits in PMCTL.
[3] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.

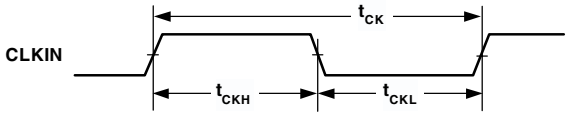


Figure 5. Clock Input

Clock Signals

The ADSP-21369 can use an external clock or a crystal. See the CLKIN pin description in Table 5. The programmer can configure the ADSP-21369 to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 6 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 16.67 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 400 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

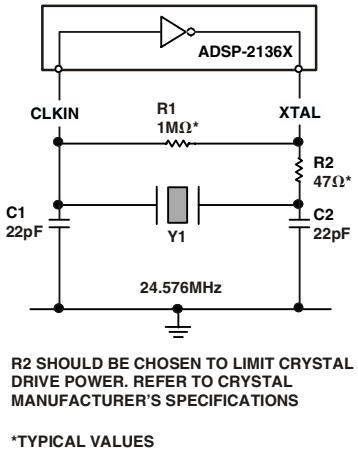


Figure 6. 400 MHz Operation (Fundamental Mode Crystal)

Reset

Table 13. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable VDD and CLKIN (not including start-up time of external clock oscillator).

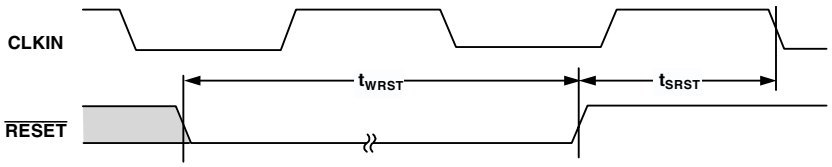


Figure 7. Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts.

Table 14. Interrupts

Parameter		Min	Max	Unit
Timing Requirement				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{PCLK} + 2$		ns

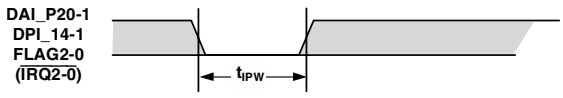


Figure 8. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (CTIMER).

Table 15. Core Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{WCTIM}	CTIMER Pulse width	$4 \times t_{PCLK} - 1$		ns

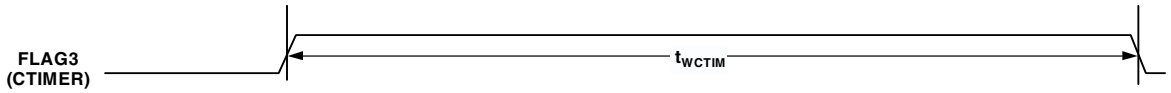


Figure 9. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0, Timer1, and Timer2 in PWM_OUT (pulse width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 16. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$2\ t_{PCLK} - 1$	$2(2^{31} - 1)\ t_{PCLK}$	ns

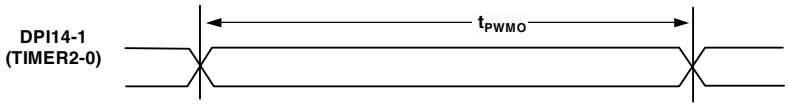


Figure 10. Timer PWM_OUT Timing

Timer WDTH_CAP Timing

The following timing specification applies to Timer0, Timer1, and Timer2 in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specification provided below are valid at the DPI_P14–1 pins.

Table 17. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{PWI}	Timer Pulse Width	2 t_{PCLK}	$2(2^{31}-1)$ t_{PCLK}	ns

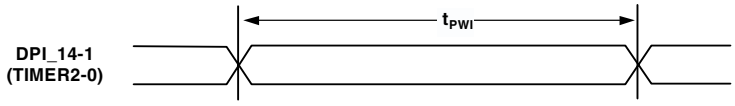


Figure 11. Timer Width Capture Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example DAI_PB01_I to DAI_PB02_O).

Table 18. DAI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI Output Valid	1.5	10	ns

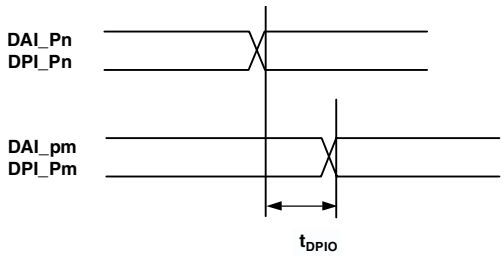


Figure 12. DAI Pin to Pin Direct Routing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the Precision Clock Generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All Timing Parameters and Switching Characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

Table 19. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIW}	Input Clock Period	24		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	2		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	2		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	2.5 + ((2.5 + D) × t_{PCGIW})	10 + ((2.5 + D) × t_{PCGIW})	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	2.5 + ((2.5 + D – PH) × t_{PCGIW})	10 + ((2.5 + D – PH) × t_{PCGIW})	ns
t_{PCGOW}	Output Clock Period	2 × t_{PCGIW}[1]		ns

D = FSxDIV, PH = FSxPHASE. For more information, see the *ADSP-2136x SHARC Processor Hardware Reference for the ADSP-21367/8/9 Processors*, "Precision Clock Generators" chapter.

[1] Normal mode of operation.

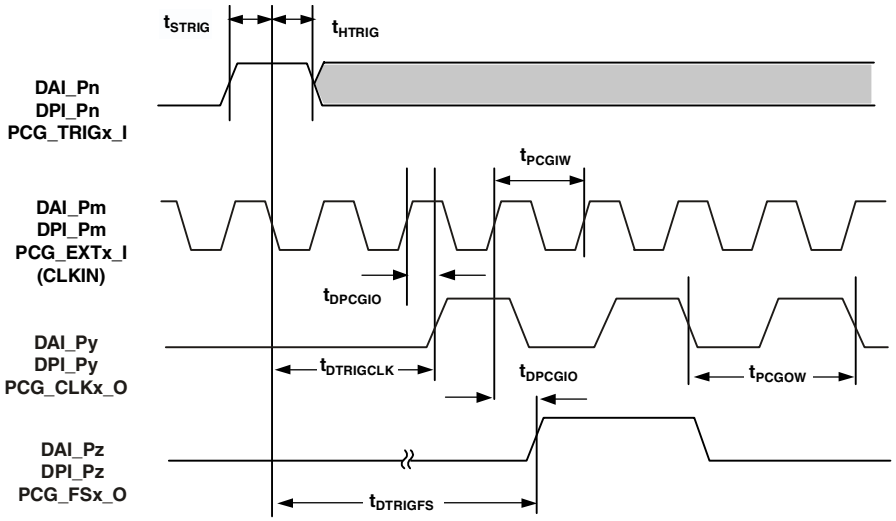


Figure 13. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to the FLAG3–0 and DPI_P14–1 pins, and the serial peripheral interface (SPI). See Table 5 for more information on flag use.

Table 20. Flags

Parameter		Min	Max	Unit
Timing Requirement				
t_{FIPW}	FLAG3–0 IN Pulse Width	$2 \times t_{PCLK} + 3$		ns
Switching Characteristic				
t_{FOPW}	FLAG3–0 OUT Pulse Width	$2 \times t_{PCLK} - 1$		ns

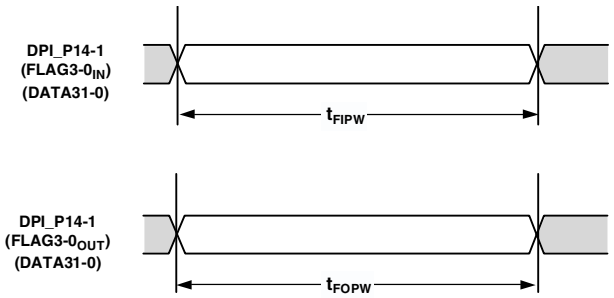


Figure 14. Flags

SDRAM Interface Timing (166 MHz SDCLK)

The 166MHz mode on the SDRAM interface is available on the 333 MHz processor only. It is not available on the 400 MHz and 266 MHz processors.

Table 21. SDRAM Interface Timing[1]

Parameter		Minimum	Maximum	Unit
Timing Requirement				
t_{SSDAT}	DATA Setup Before SDCLK	0		ns
t_{HSDAT}	DATA Hold After SDCLK	1.0		ns
Switching Characteristic				
t_{SCLK}	SDCLK Period	6.0		ns
t_{SCLKH}	SDCLK Width High	2.9		ns
t_{SCLKL}	SDCLK Width Low	2.9		ns
t_{DCAD}	Command, ADDR, Data Delay After SDCLK[2]		4.0	ns
t_{HCAD}	Command, ADDR, Data Hold After SDCLK[2]	1.47		ns
t_{DSDAT}	Data Disable After SDCLK		5.3	ns
t_{ENSDAT}	Data Enable After SDCLK	2.6		ns

[1] For F_{CCLK} = 333 MHz (SDCK ratio 1:2).
[2] Command pins include: $\overline{SDCAS}$, $\overline{SDRAS}$, $\overline{SDWE}$, $\overline{MSx}$, SDA10, SDCKE.

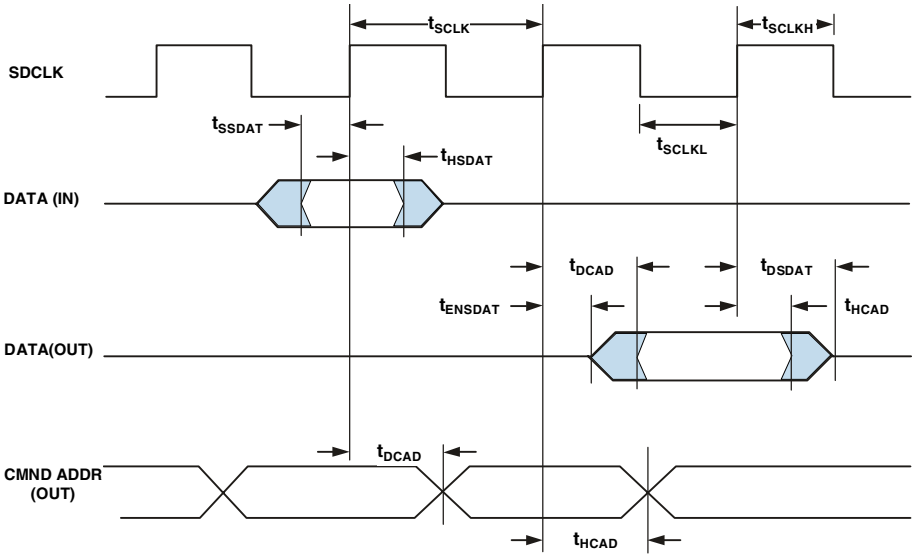


Figure 15. SDRAM Interface Timing for 166 MHz SDCLK

SDRAM Interface Timing (133 MHz SDCLK)

Table 22. SDRAM Interface Timing[1]

Parameter		Minimum	Maximum	Unit
Timing Requirement				
t_{SSDAT}	DATA Setup Before SDCLK	0.0		ns
t_{HSDAT}	DATA Hold After SDCLK	1.0		ns
Switching Characteristic				
t_{SCLK}	SDCLK Period	7.5		ns
t_{SCLKH}	SDCLK Width High	3.65		ns
t_{SCLKL}	SDCLK Width Low	3.65		ns
t_{DCAD}	Command, ADDR, Data Delay After SDCLK[2]		4.0	ns
t_{HCAD}	Command, ADDR, Data Hold After SDCLK[2]	1.5		ns
t_{DSDAT}	Data Disable After SDCLK		5.3	ns
t_{ENSDAT}	Data Enable After SDCLK	2.6		ns

[1] For F_{CCLK} = 400 MHz (SDCK ratio = 1:3).
[2] Command pins include: $\overline{SDCAS}$, $\overline{SDRAS}$, $\overline{SDWE}$, $\overline{MSx}$, SDA10, SDCKE.

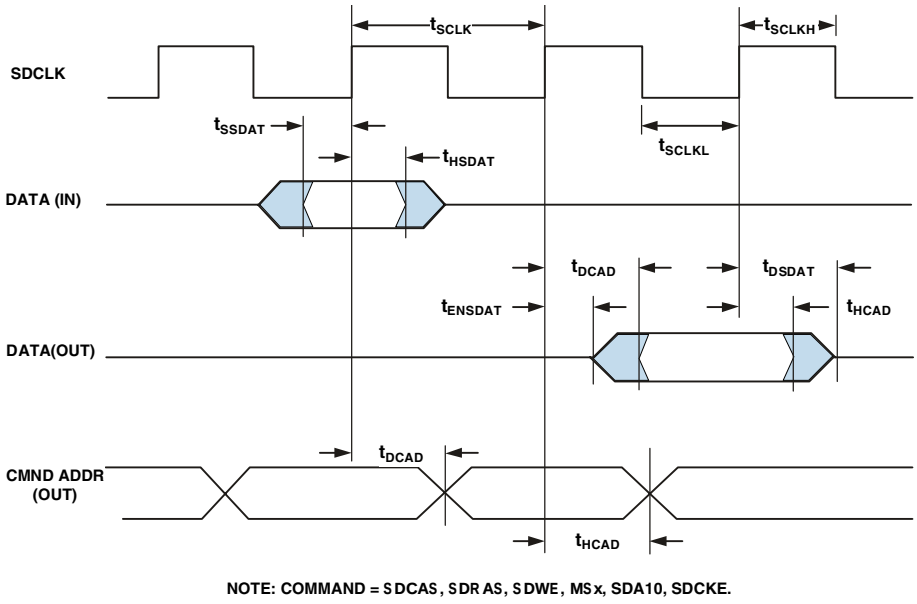


Figure 16. SDRAM Interface Timing for 133 MHz SDCLK

Memory Read – Bus Master

Use these specifications for asynchronous interfacing to memories. These specifications apply when the ADSP-21369 is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.

Table 23. Memory Read – Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		W+t_{SDCK}–5.12	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		W– 1.5 + t_{SDCK}	ns
t_{SDS}	Data Setup to $\overline{RD}$ High	1.79		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3, 4]	0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 5]		t_{SDCK}–9.5+ W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[4]		W– 7.0	ns
t_{HAKC}	ACK Hold After $\overline{RD}$ High	0		ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High	RH + 0.44		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[2]	t_{SDCK}–3.3		ns
t_{RW}	$\overline{RD}$ Pulsewidth	W – 0.5		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, Low	HI +t_{SDCK}–1		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCK}.
HI =RHC + IC (RHC = (number of Read Hold Cycles specified in AMICTLx register) x t_{SDCK}
IC = (number of Idle Cycles specified in AMICTLx register) x t_{SDCK}).
H = (number of Hold Cycles specified in AMICTLx register) x t_{SDCK}.

[1] Data Delay/Setup: User must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{MS}$x, is referenced.
[3] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.
[4] Data Hold: User must meet t_{HDA} or t_{HDRH} in asynchronous access mode. See Test Conditions on Page 46 for the calculation of hold times given capacitive and dc loads.
[5] ACK Delay/Setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (Low). For asynchronous assertion of ACK (High) user must meet t_{DAAK} or t_{DSAK}.

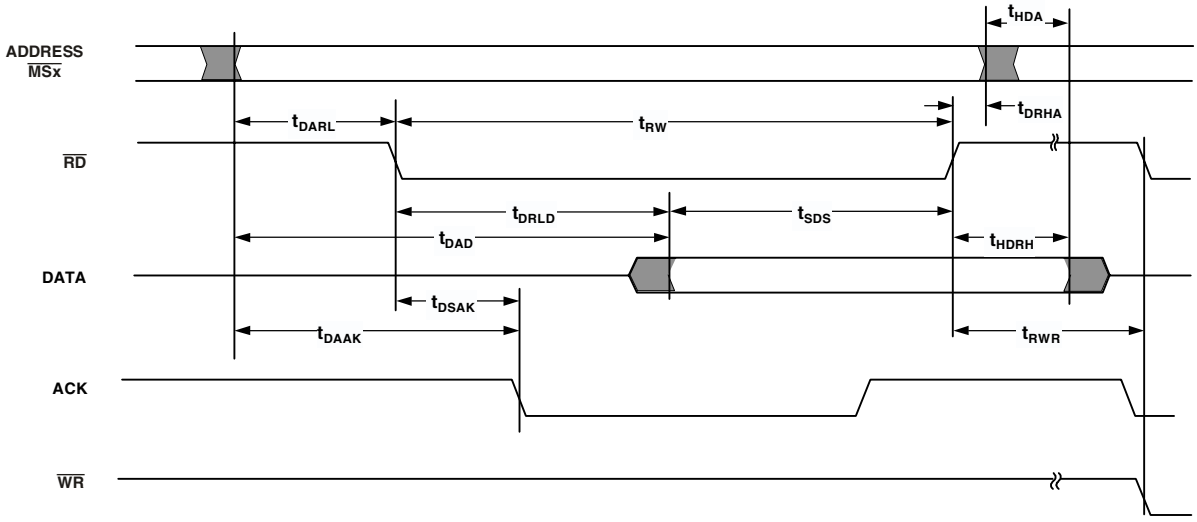


Figure 17. Memory Read – Bus Master

Memory Write – Bus Master

Use these specifications for asynchronous interfacing to memories. These specifications apply when the ADSP-21369 is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.

Table 24. Memory Write – Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		t_{SDCK} – 9.7 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low [1, 3]		W – 7.1	ns
t_{HAKC}	ACK Hold After $\overline{WR}$ High[1]	0		ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	t_{SDCK} – 3.1 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	t_{SDCK} – 2.7		ns
t_{WW}	$\overline{WR}$ Pulsewidth	W – 0.4		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	t_{SDCK} – 2.1 + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	H + 0.3		ns
t_{DWHD}	Data Hold After $\overline{WR}$ Deasserted	H + 0.4		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[4]	t_{SDCK} – 1.37 + H	t_{SDCK} + 3.9 + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$ Low	t_{SDCK} – 0.2 + H		ns
t_{DDWR}	Data Disable Before $\overline{RD}$ Low	$2t_{SDCK}$ – 4.11		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	t_{SDCK} – 3.5		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCK}.
H = (number of hold cycles specified in AMICTLx register) x t_{SDCK}.

[1] ACK Delay/Setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (Low). For asynchronous assertion of ACK (High) user must meet t_{DAAK} or t_{DSAK}.
[2] The falling edge of $\overline{MSx}$ is referenced.
[3] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only applies to asynchronous access mode.
[4] See Test Conditions on Page 46 for calculation of hold times given capacitive and dc loads.

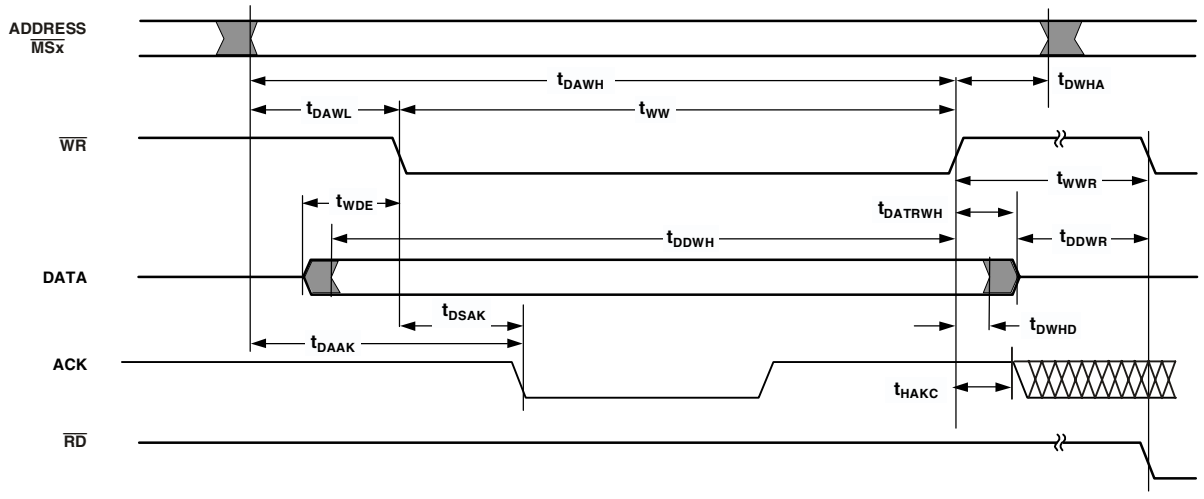


Figure 18. Memory Write – Bus Master

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Serial port signals (SCLK, FS, data channel A, data channel B) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 25. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}[1]	FS Setup Before SCLK (Externally Generated FS in either Transmit or Receive Mode)	2.5		ns
t_{HFSE}[1]	FS Hold After SCLK (Externally Generated FS in either Transmit or Receive Mode)	2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	2.5		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		ns
t_{SCLKW}	SCLK Width	10		ns
t_{SCLK}	SCLK Period	20		ns
Switching Characteristics				
t_{DFSE}[2]	FS Delay After SCLK (Internally Generated FS in either Transmit or Receive Mode)		7	ns
t_{HOFSE}[2]	FS Hold After SCLK (Internally Generated FS in either Transmit or Receive Mode)	2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		7	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 26. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}[1]	FS Setup Before SCLK (Externally Generated FS in either Transmit or Receive Mode)	7		ns
t_{HFSI}[1]	FS Hold After SCLK (Externally Generated FS in either Transmit or Receive Mode)	2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		ns
Switching Characteristics				
t_{DFSI}[2]	FS Delay After SCLK (Internally Generated FS in Transmit Mode)		3	ns
t_{HOFSI}[2]	FS Hold After SCLK (Internally Generated FS in Transmit Mode)	–1.0		ns
t_{DFSI}[2]	FS Delay After SCLK (Internally Generated FS in Receive or Mode)		3	ns
t_{HOFSI}[2]	FS Hold After SCLK (Internally Generated FS in Receive Mode)	–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0		ns
t_{SCLKIW}	Transmit or Receive SCLK Width	$0.5t_{SCLK} - 2$	$0.5t_{SCLK} + 2$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

Table 27. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	2		ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK		7	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	–1		ns

[1] Referenced to drive edge.

Table 28. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0		7	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to Left-justified Sample Pair as well as DSP serial mode, and MCE = 1, MFD = 0.

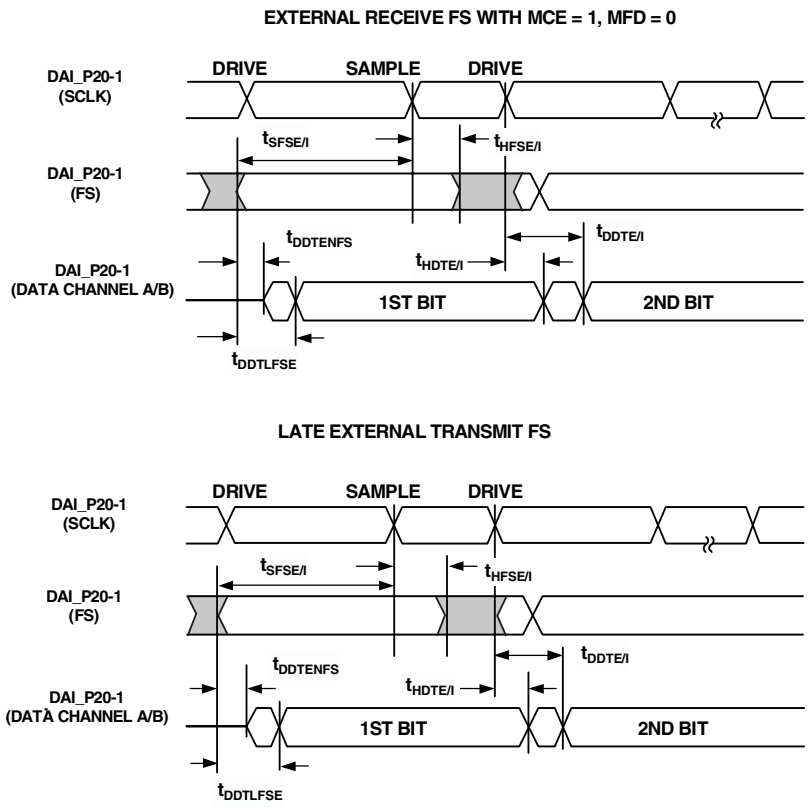


Figure 19. External Late Frame Sync[1]

[1] This figure reflects changes made to support Left-justified Sample Pair mode.

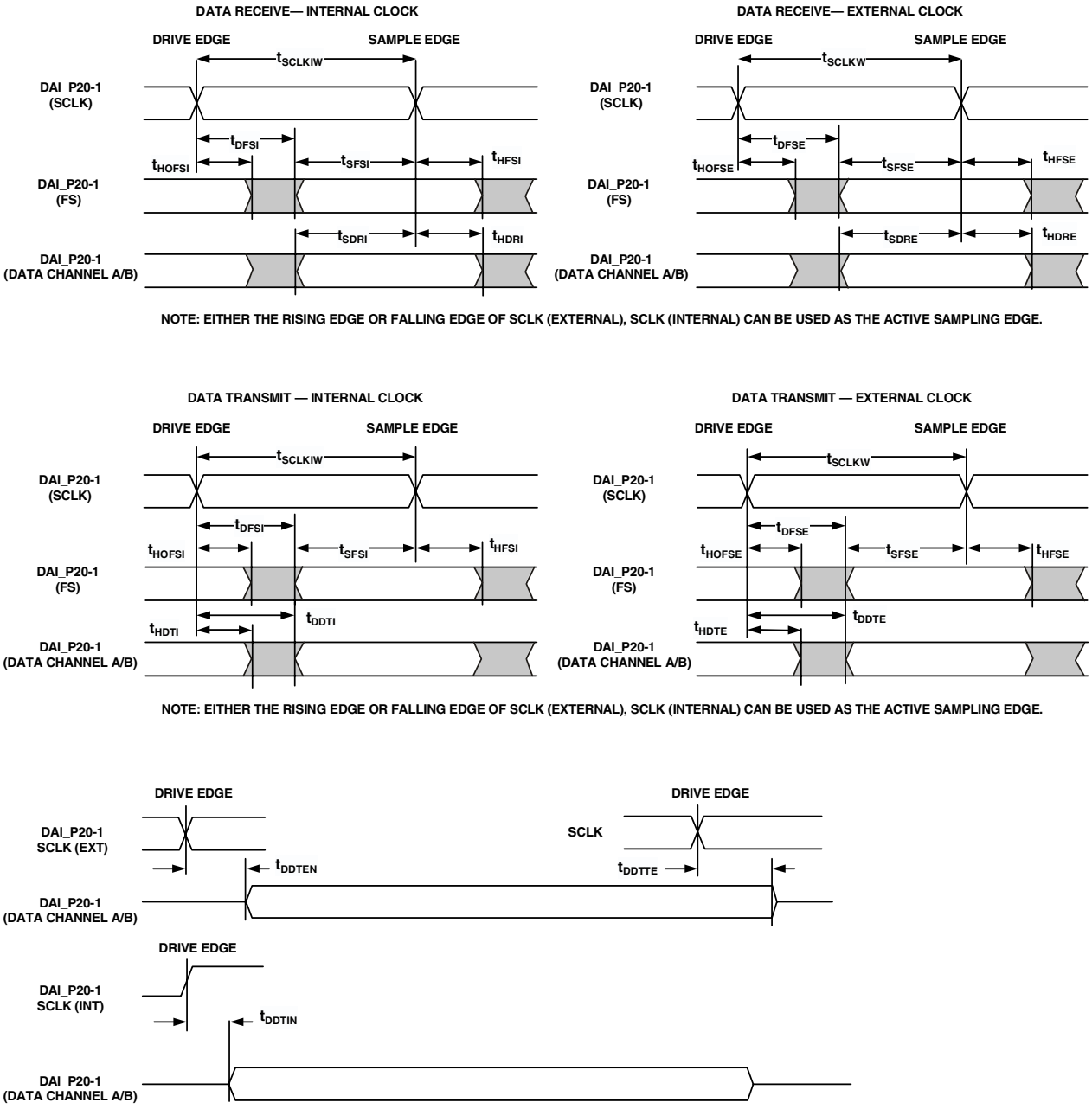


Figure 20. Serial Ports

Input Data Port

The timing requirements for the IDP are given in Table 29.IDP Signals (SCLK, FS, SDATA) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 29. IDP

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	FS Setup Before SCLK Rising Edge	2.5		ns
t_{SIHFS}[1]	FS Hold After SCLK Rising Edge	2.5		ns
t_{SISD}[1]	SData Setup Before SCLK Rising Edge	2.5		ns
t_{SIHD}[1]	SData Hold After SCLK Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	9		ns
t_{IDPCLK}	Clock Period	24		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

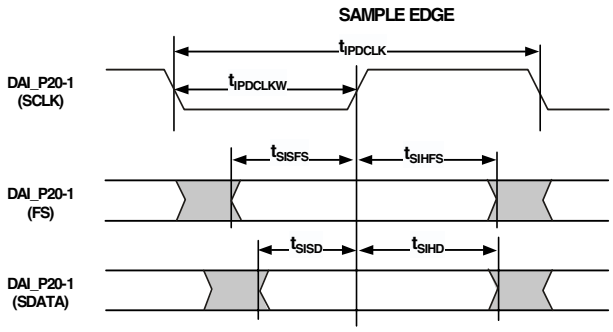


Figure 21. IDP Master Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 30. PDAP is the parallel mode operation of channel 0 of the IDP. For details on the operation of the IDP, see the IDP chapter of the *ADSP-2136x SHARC Processor Hardware Reference for the ADSP-21367/8/9 Processors*. Note that the most significant 16 bits of external PDAP data can be provided through the DATA31–16 pins. The remaining 4 bits can only be sourced through DAI_P4–1. The timing below is valid at the DATA31–16 pins.

Table 30. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPCLKEN}$[1]	PDAP_CLKEN Setup Before PDAP_CLK Sample Edge	2.5		ns
$t_{HPCLKEN}$[1]	PDAP_CLKEN Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge	2.5		ns
t_{PDHD}[1]	PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge	2.5		ns
t_{PDCLKW}	Clock Width	7		ns
t_{PDCLK}	Clock Period	24		ns
Switching Characteristics				
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} - 1$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1$		ns

[1] Source pins of DATA are ADDR7–0, DATA7–0, or DAI pins. Source pins for SCLK and FS are: 1) DAI pins, 2) CLKIN through PCG, or 3) DAI pins through PCG.

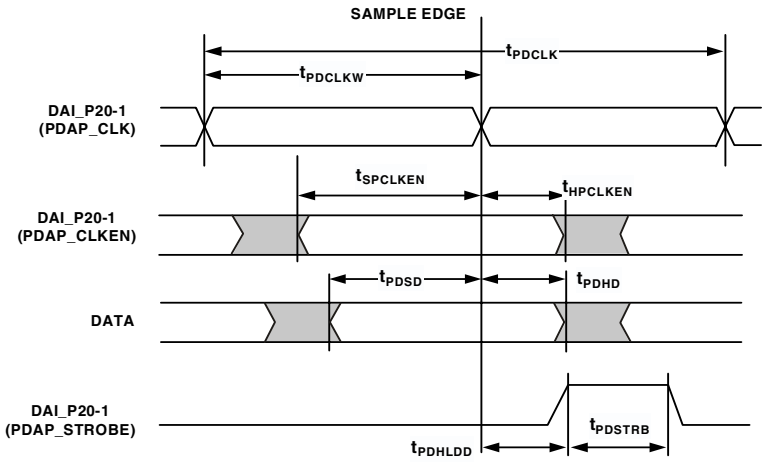


Figure 22. PDAP Timing

Pulse Width Modulation Generators

Table 31. PWM Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2$	$2^{16} - 2) \times t_{PCLK} - 2$	ns
t_{WCTIM}	PWM Output Period	$2 \times t_{PCLK}$	$(2^{16} - 1) \times t_{PCLK}$	ns

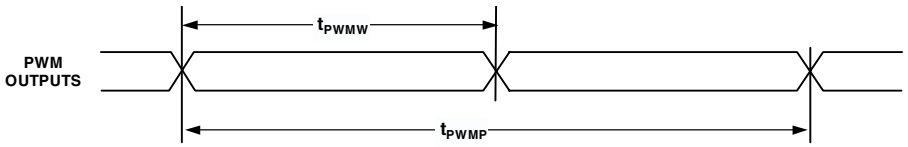


Figure 23. PWM Timing

Sample Rate Converter—Serial Input Port

The SRC input signals (SCLK, FS, and SDATA) are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 32 are valid at the DAI_P20–1 pins.

Table 32. SRC, Serial Input Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SRCHFS}[1]	FS Hold After SCLK Rising Edge	5.5		ns
t_{SRCSD}[1]	SData Setup Before SCLK Rising Edge	4		ns
t_{SRCHD}[1]	SData Hold After SCLK Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	9		ns
t_{SRCCLK}	Clock Period	20		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

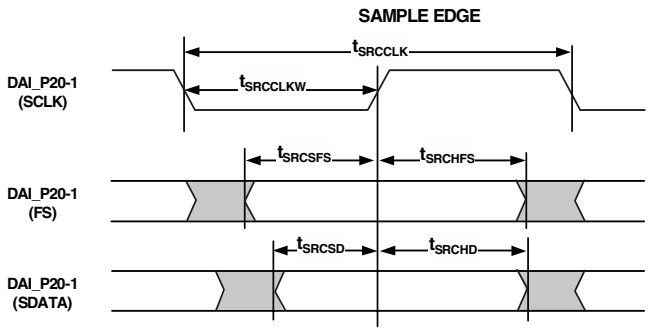


Figure 24. SRC Serial Input Port Timing

Sample Rate Converter—Serial Output Port

For the serial output port, the frame-sync is an input and it should meet setup and hold times with regard to SCLK on the output port. The serial data output, SDATA, has a hold time and delay specification with regard to SCLK. Note that SCLK rising edge is the sampling edge and the falling edge is the drive edge.

Table 33. SRC, Serial Output Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SRCHFS}[1]	FS Hold Before SCLK Rising Edge	5.5		ns
Switching Characteristics				
t_{SRCTDD}[1]	Transmit Data Delay After SCLK Falling Edge		7	ns
t_{SRCTDH}[1]	Transmit Data Hold After SCLK Falling Edge	2		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

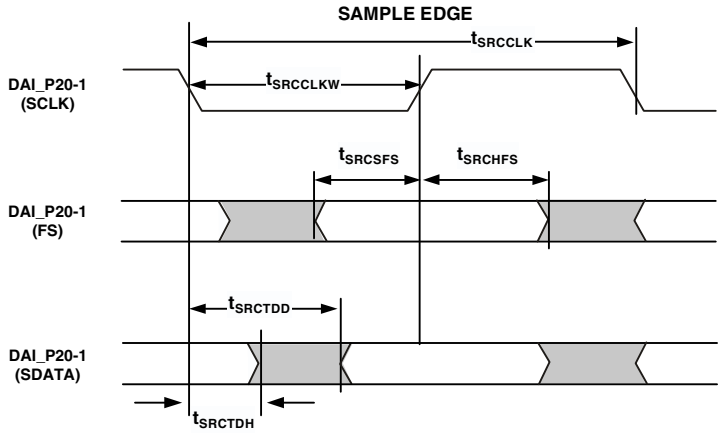


Figure 25. SRC Serial Output Port Timing

SPDIF Transmitter

Serial data input to the SPDIF transmitter can be formatted as left justified, I²S or right justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

SPDIF Transmitter—Serial Input Waveforms

Figure 26 shows the right-justified mode. LRCLK is HI for the left channel and LO for the right channel. Data is valid on the rising edge of SCLK. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output mode) from an LRCLK transition, so that when there are 64 SCLK periods per LRCLK period, the LSB of the data will be right-justified to the next LRCLK transition.

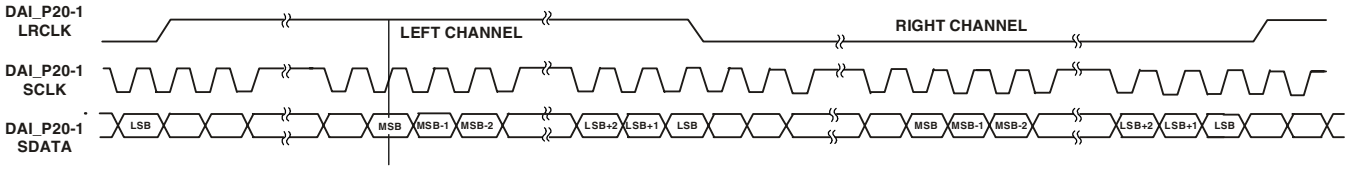


Figure 26. Right-Justified Mode

Figure 27 shows the default I²S-justified mode. LRCLK is LO for the left channel and HI for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition but with a single SCLK period delay.

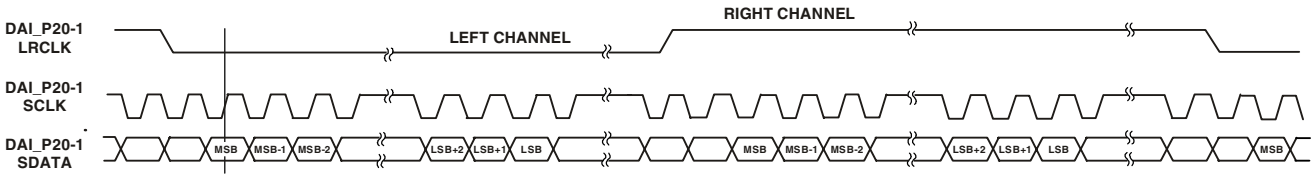


Figure 27. I²S-Justified Mode

Figure 28 shows the left-justified mode. LRCLK is HI for the left channel and LO for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition with no MSB delay.

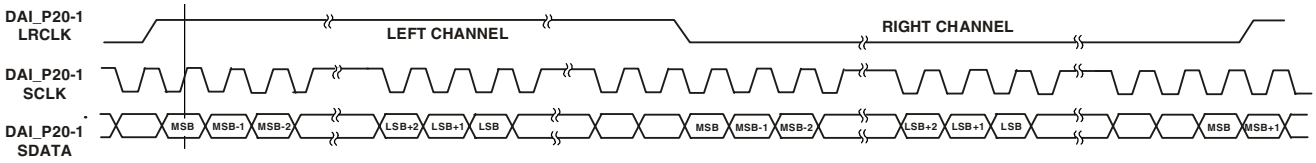


Figure 28. Left-Justified Mode

SPDIF Transmitter Input Data Timing

The timing requirements for the Input port are given in Table 34. Input Signals (SCLK, FS, SDATA) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 34. SPDIF Transmitter Input Data Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SIFS}[1]	FS Setup Before SCLK Rising Edge	4		ns
t_{SIHFS}[1]	FS Hold After SCLK Rising Edge	5.5		ns
t_{SISD}[1]	SData Setup Before SCLK Rising Edge	4		ns
t_{SIHD}[1]	SData Hold After SCLK Rising Edge	5.5		ns
$t_{SISCLKW}$	Clock Width	36		ns
t_{SISCLK}	Clock Period	80		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		ns
$t_{SITXCLK}$	Transmit Clock Period	20		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

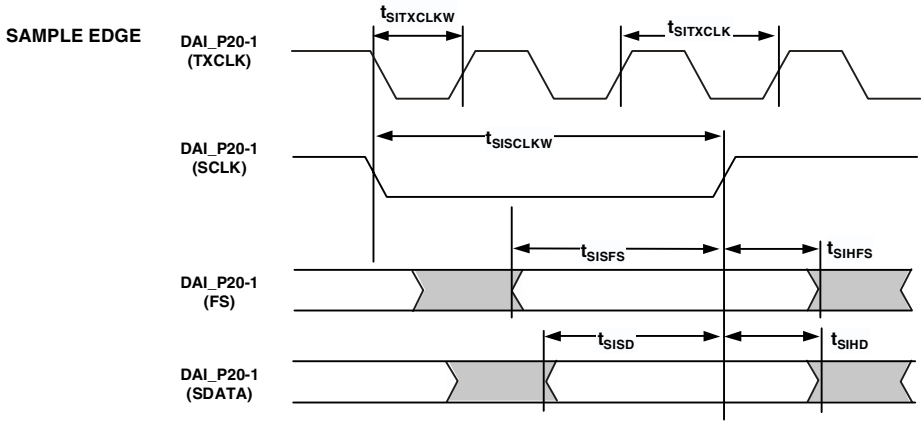


Figure 29. SPDIF Transmitter Input Timing

Over Sampling Clock (TXCLK) Switching Characteristics

The SPDIF transmitter has an over sampling clock. This TXCLK input is divided down to generate the biphase clock.

Table 35. Over Sampling Clock (TXCLK) Switching Characteristics

Parameter	Min	Max	Unit
TXCLK Frequency for TXCLK = 768 × FS		147.5	MHz
TXCLK Frequency for TXCLK = 512 × FS		98.4	MHz
TXCLK Frequency for TXCLK = 384 × FS		73.8	MHz
TXCLK Frequency for TXCLK = 256 × FS		49.2	MHz
Frame Rate		192.0	kHz

SPDIF Receiver

The following section describes timing as it relates to the SPDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the 512 × Fs clock.

Table 36. SPDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	LRCLK Delay After SCLK		5	ns
t_{HOFSI}	LRCLK Hold After SCLK	–2		ns
t_{DDTI}	Transmit Data Delay After SCLK		5	ns
t_{HDTI}	Transmit Data Hold After SCLK	–2		ns
t_{SCLKIW}[1]	Transmit SCLK Width	40		ns
t_{CCLK}	Core Clock Period		5	ns

[1] SCLK frequency is 64 x FS where FS = the frequency of LRCLK.

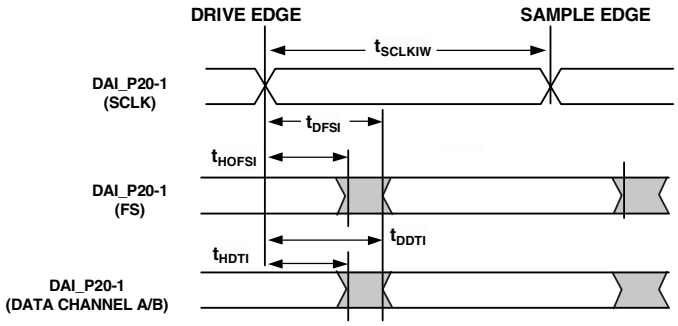


Figure 30. SPDIF Receiver Internal Digital PLL Mode Timing

SPI Interface—Master

The ADSP-21369 contains two SPI ports. The primary has dedicated pins and the secondary is available through the DPI. The timing provided in Table 37 and Table 38 on page 42 applies to both.

Table 37. SPI Interface Protocol — Master Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid To SPICLK Edge (Data Input Set-up Time)	8		ns
t_{HSPIDM}	SPICLK Last Sampling Edge To Data Input Not Valid	2		ns
Switching Characteristics				
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK}$		ns
t_{SPICHM}	SErial Clock High Period	$4 \times t_{PCLK}$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		0	
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	2		ns
t_{SDSCIM}	FLAG3–0IN (SPI device select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to FLAG3–0IN High	$4 \times t_{PCLK} - 1$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1$		ns

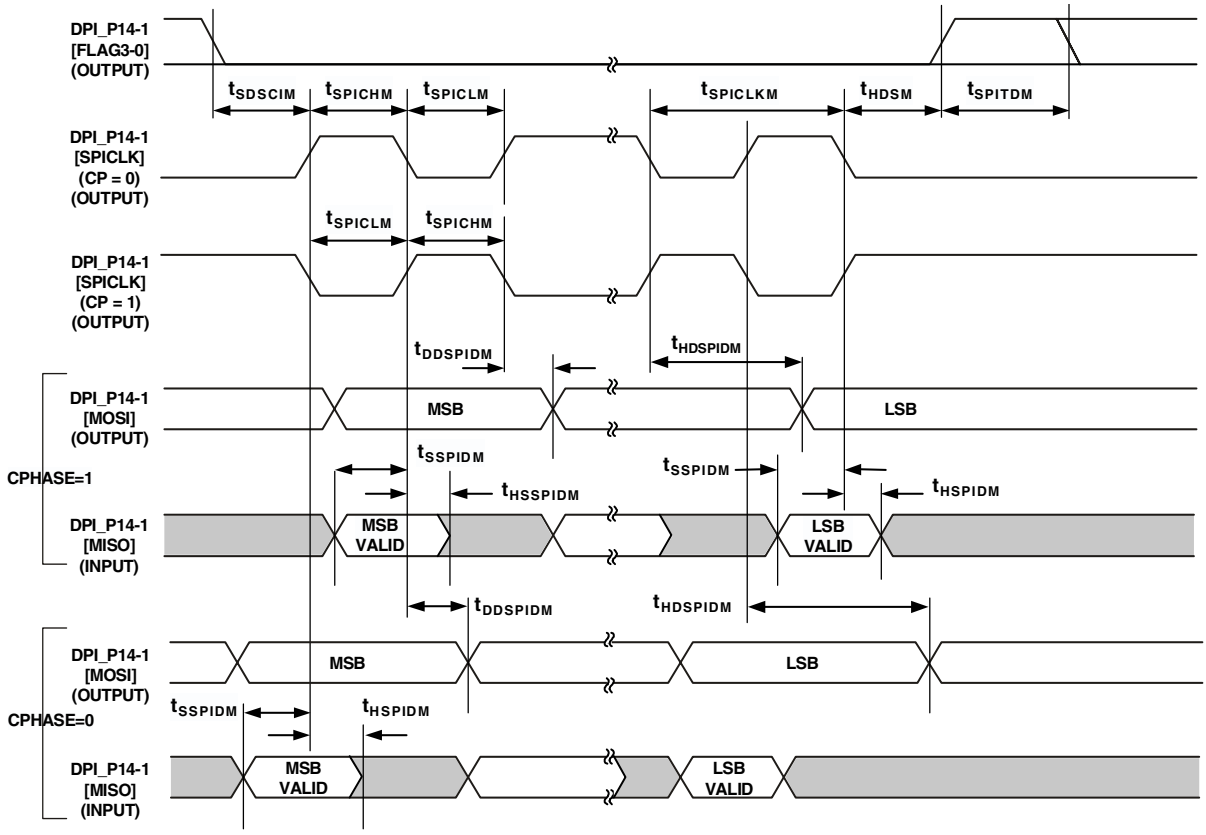


Figure 31. SPI Master Timing

SPI Interface—Slave

Table 38. SPI Interface Protocol —Slave Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK}$		ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK}$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$		ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge			ns
	CPHASE = 0	$2 \times t_{PCLK}$		
	CPHASE = 1	$2 \times t_{PCLK}$		
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	$2 \times t_{PCLK}$		ns
t_{SSPIDS}	Data Input Valid to SPICLK edge (Data Input Set-up Time)	2		ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE=0)	$2 \times t_{PCLK}$		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	4	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	4	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		9.4	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{PCLK}$		ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE=0)		$5 \times t_{PCLK}$	ns

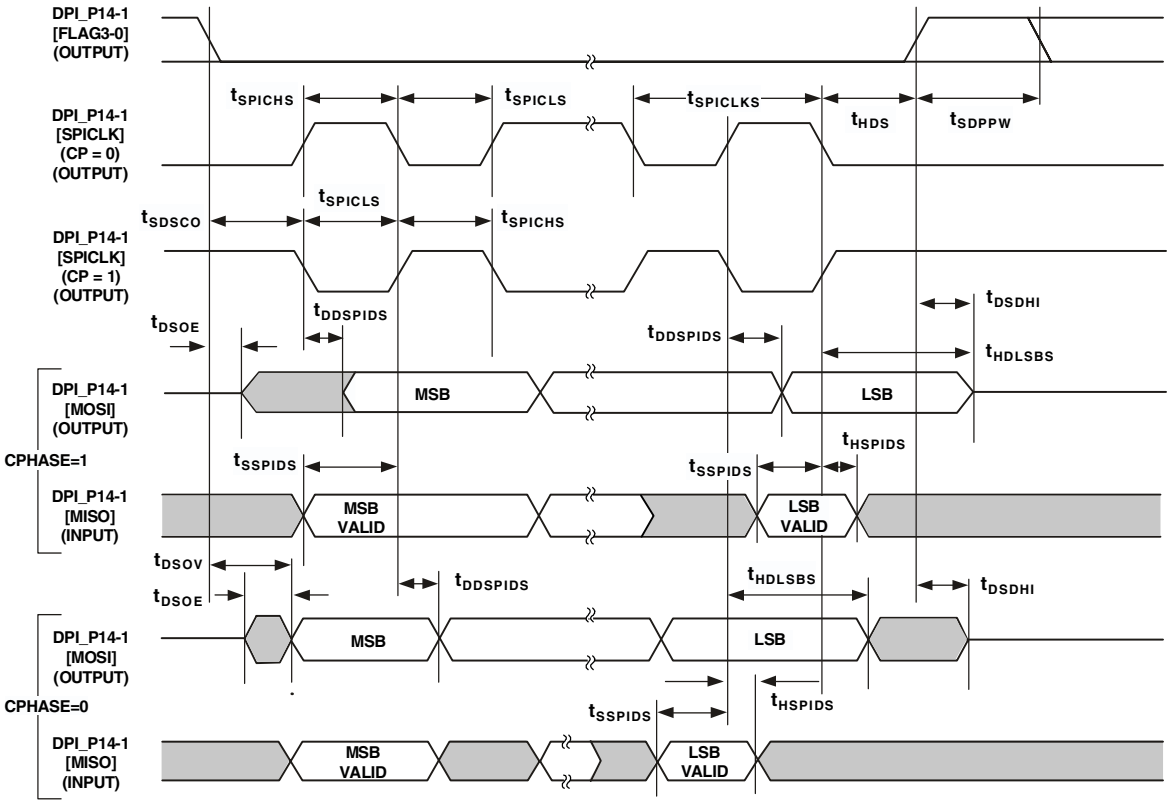


Figure 32. SPI Slave Timing

Universal Asynchronous Receiver-Transmitter (UART) Port—Receive and Transmit Timing

Figure 33 describes UART port receive and transmit operations. The maximum baud rate is SCLK/16. As shown in Figure 33 there is some latency between the generation internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART.

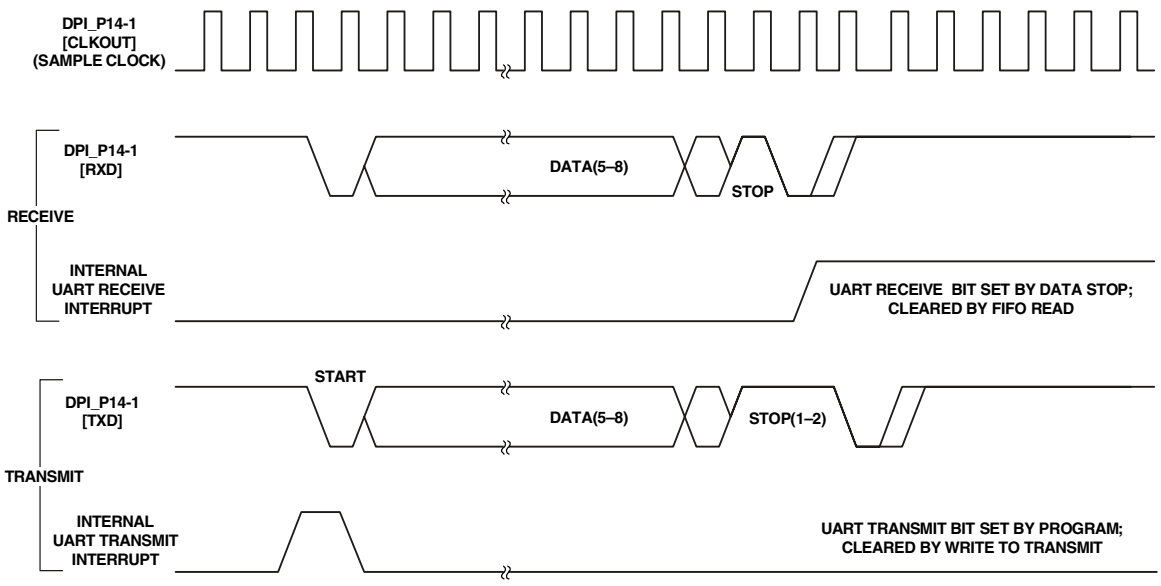


Figure 33. UART Port—Receive and Transmit Timing

TWI Controller Timing

Table 39 and Figure 34 provide timing information for the TWI interface. Input Signals (SCL, SDA) are routed to the DPI_P14–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 39. Characteristics of the SDA and SCL Bus Lines for F/S-Mode TWI Bus Devices[1]

Parameter		Standard-mode		Fast-mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	0	100	0	400	kHz
t_{HDSTA}	Hold Time (repeated) START Condition. After this Period, the First Clock Pulse is Generated.	4.0		0.6		µs
t_{LOW}	LOW Period of the SCL Clock	4.7		1.3		µs
t_{HIGH}	HIGH period of the SCL Clock	4.0		0.6		µs
t_{SUSTA}	Set-up time for a repeated START condition	4.7		0.6		µs
t_{HDDAT}	Data Hold Time for TWI-bus Devices	0		0		µs
t_{SUDAT}	Data Set-up Time	250		100		ns
t_{SUSTO}	Set-up Time for STOP Condition	4.0		0.6		µs
t_{BUF}	Bus Free Time Between a STOP and START Condition	4.7		1.3		µs
t_{SP}	Pulse Width of Spikes Suppressed By the Input Filter	n/a	n/a	0	50	ns

[1] All values referred to V_{IHmin} and V_{ILmax} levels. For more information, see Electrical Characteristics on page 16.

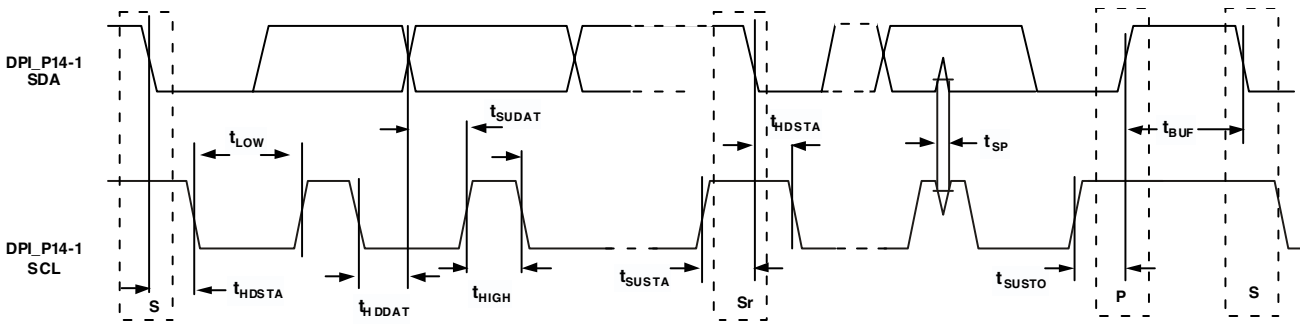


Figure 34. Fast and Standard Mode Timing on the TWI Bus

JTAG Test Access Port and Emulation

Table 40. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = AD15–0, $\overline{\text{SPIDS}}$, CLKCFG1–0, $\overline{\text{RESET}}$, BOOTCFG1–0, MISO, MOSI, SPICLK, DAI_Px, FLAG3–0.
[2] System Outputs = MISO, MOSI, SPICLK, DAI_Px, AD15–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, FLAG3–0, CLKOUT, $\overline{\text{EMU}}$, ALE.

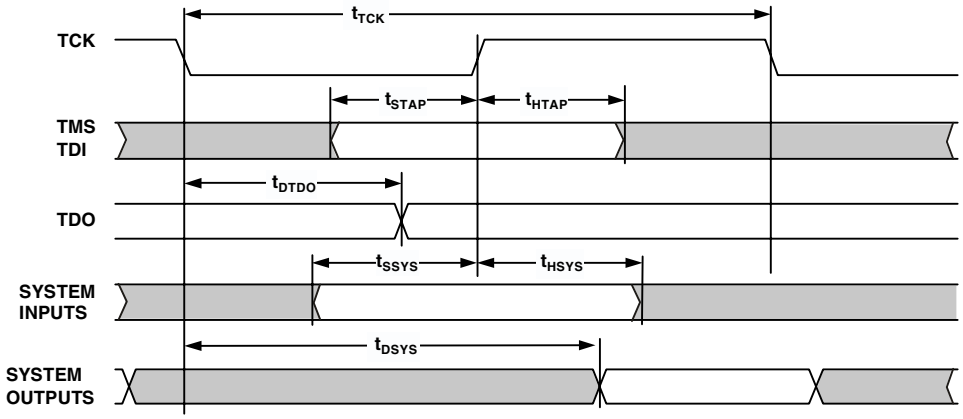


Figure 35. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 36 shows typical I-V characteristics for the output drivers of the ADSP-21369. The curves represent the current drive capability of the output drivers as a function of output voltage.

TBD

Figure 36. ADSP-21369 Typical Drive

TEST CONDITIONS

The ac signal specifications (timing parameters) appear Table 13 on page 21 through Table 40 on page 45. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 37.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 38. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

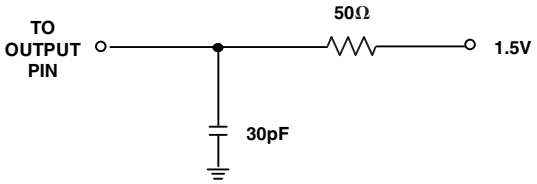


Figure 37. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

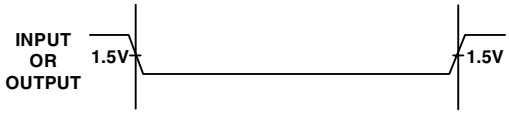


Figure 38. Voltage Reference Levels for AC Measurements

THERMAL CHARACTERISTICS

The ADSP-21369 processor is rated for performance over the temperature range specified in Recommended Operating Conditions on Page 16.

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 37). Figure 41 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 39, Figure 40, and Figure 41 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20%-80%, V=Min) vs. Load Capacitance.

TBD

Figure 39. Typical Output Rise/Fall Time (20%-80%, V_{DDEXT} = Max)

TBD

Figure 40. Typical Output Rise/Fall Time (20%-80%, V_{DDEXT} =Min)

TBD

Figure 41. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

Table 41 and Table 42 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-9 (SBGA) and JESD51-7 (MQFP). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the Junction Temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature °C

T_{CASE} = Case temperature (°C) measured at the top center of the package

Ψ_{JT} = Junction-to-Top (of package) characterization parameter is the Typical value from Table 41 and Table 42.

P_D = Power dissipation (see EE Note #TBD)

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient Temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations. Note that the thermal characteristics values provided in Table 41 and Table 42 are modeled values.

Table 41. Thermal Characteristics for 256 Ball SBGA (No thermal vias in PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	12.5	°C/W
θ_{JMA}	Airflow = 1 m/s	10.6	°C/W
θ_{JMA}	Airflow = 2 m/s	9.9	°C/W
θ_{JC}		0.7	°C/W
θ_{JB}		5.3	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.3	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.3	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.3	°C/W

Table 42. Thermal Characteristics for 208-Lead MQFP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	25.0	°C/W
θ_{JMA}	Airflow = 1 m/s	22.5	°C/W
θ_{JMA}	Airflow = 2 m/s	21.6	°C/W
θ_{JC}		9.6	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.7	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.8	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.9	°C/W

256-BALL SBGA PINOUT

Table 43. 256-Ball SBGA Pin Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A01	NC	B01	DAI5	C01	DAI9	D01	DAI10
A02	TDI	B02	SDCLK1	C02	DAI7	D02	DAI6
A03	TMS	B03	$\overline{\text{TRST}}$	C03	GND	D03	GND
A04	CLK_CFG0	B04	TCK	C04	IOVDD	D04	IOVDD
A05	CLK_CFG1	B05	BOOTCFG_0	C05	GND	D05	GND
A06	$\overline{\text{EMU}}$	B06	BOOTCFG_1	C06	GND	D06	IOVDD
A07	DAI4	B07	TDO	C07	VDD	D07	VDD
A08	DAI1	B08	DAI3	C08	GND	D08	GND
A09	DPI14	B09	DAI2	C09	GND	D09	IOVDD
A10	DPI12	B10	DPI13	C10	VDD	D10	VDD
A11	DPI10	B11	DPI11	C11	GND	D11	GND
A12	DPI9	B12	DPI8	C12	GND	D12	IOVDD
A13	DPI7	B13	DPI5	C13	VDD	D13	VDD
A14	DPI6	B14	DPI4	C14	GND	D14	GND
A15	DPI3	B15	DPI1	C15	GND	D15	IOVDD
A16	DPI2	B16	$\overline{\text{RESET}}$	C16	VDD	D16	GND
A17	CLKOUT	B17	DATA30	C17	VDD	D17	IOVDD
A18	DATA31	B18	DATA29	C18	VDD	D18	GND
A19	NC	B19	DATA28	C19	DATA27	D19	DATA26
A20	NC	B20	NC	C20	NC	D20	DATA24
E01	DAI11	F01	DAI14	G01	DAI15	H01	DAI17
E02	DAI8	F02	DAI12	G02	DAI13	H02	DAI16
E03	VDD	F03	GND	G03	GND	H03	VDD
E04	VDD	F04	GND	G04	IOVDD	H04	VDD
E17	GND	F17	IOVDD	G17	VDD	H17	IOVDD
E18	GND	F18	GND	G18	VDD	H18	GND
E19	DATA25	F19	GND	G19	DATA22	H19	DATA19
E20	DATA23	F20	DATA21	G20	DATA20	H20	DATA18
J01	DAI19	K01	FLAG0	L01	FLAG2	M01	ACK
J02	DAI18	K02	DAI20	L02	FLAG1	M02	FLAG3
J03	GND	K03	GND	L03	VDD	M03	GND
J04	GND	K04	IOVDD	L04	VDD	M04	GND

Table 43. 256-Ball SBGA Pin Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
J17	GND	K17	VDD	L17	VDD	M17	IOVDD
J18	GND	K18	VDD	L18	VDD	M18	GND
J19	GND	K19	GND	L19	DATA15	M19	DATA12
J20	DATA17	K20	DATA16	L20	DATA14	M20	DATA13
N01	$\overline{RD}$	P01	SDA10	R01	$\overline{SDWE}$	T01	SDCKE
N02	SDCLK0	P02	$\overline{WR}$	R02	$\overline{SDRAS}$	T02	$\overline{SDCAS}$
N03	GND	P03	VDD	R03	GND	T03	GND
N04	IOVDD	P04	VDD	R04	GND	T04	IOVDD
N17	GND	P17	VDD	R17	IOVDD	T17	GND
N18	GND	P18	VDD	R18	GND	T18	GND
N19	DATA11	P19	DATA8	R19	DATA6	T19	DATA5
N20	DATA10	P20	DATA9	R20	DATA7	T20	DATA4
U01	$\overline{MS0}$	V01	ADDR22	W01	GND	Y01	GND
U02	$\overline{MS1}$	V02	ADDR23	W02	ADDR21	Y02	NC
U03	VDD	V03	VDD	W03	ADDR19	Y03	NC
U04	GND	V04	GND	W04	ADDR20	Y04	ADDR18
U05	IOVDD	V05	GND	W05	ADDR17	Y05	NC
U06	GND	V06	GND	W06	ADDR16	Y06	NC
U07	IOVDD	V07	GND	W07	ADDR15	Y07	XTAL2
U08	VDD	V08	VDD	W08	ADDR14	Y08	CLKIN
U09	IOVDD	V09	GND	W09	AVDD	Y09	NC
U10	GND	V10	GND	W10	AVSS	Y10	NC
U11	IOVDD	V11	GND	W11	ADDR13	Y11	NC
U12	VDD	V12	VDD	W12	ADDR12	Y12	NC
U13	IOVDD	V13	IOVDD	W13	ADDR10	Y13	ADDR11
U14	IOVDD	V14	GND	W14	ADDR8	Y14	ADDR9
U15	VDD	V15	VDD	W15	ADDR5	Y15	ADDR7
U16	IOVDD	V16	GND	W16	ADDR4	Y16	ADDR6
U17	VDD	V17	GND	W17	ADDR1	Y17	ADDR3
U18	VDD	V18	GND	W18	ADDR2	Y18	GND
U19	DATA0	V19	DATA1	W19	ADDR0	Y19	GND
U20	DATA2	V20	DATA3	W20	NC	Y20	NC

208-LEAD MQFP PINOUT

Table 44. 208-Lead MQFP Pin Assignment (Numerically by Lead Number)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	VDD	53	VDD	105	VDD	157	VDD
2	DATA28	54	GND	106	GND	158	VDD
3	DATA27	55	IOVDD	107	IOVDD	159	GND
4	GND	56	ADDR0	108	$\overline{\text{SDCAS}}$	160	VDD
5	IOVDD	57	ADDR2	109	$\overline{\text{SDRAS}}$	161	VDD
6	DATA26	58	ADDR1	110	SDCKE	162	VDD
7	DATA25	59	ADDR4	111	$\overline{\text{SDWE}}$	163	TDI
8	DATA24	60	ADDR3	112	$\overline{\text{WR}}$	164	$\overline{\text{TRST}}$
9	DATA23	61	ADDR5	113	SDA10	165	TCK
10	GND	62	GND	114	GND	166	GND
11	VDD	63	VDD	115	IOVDD	167	VDD
12	DATA22	64	GND	116	SDCLK0	168	TMS
13	DATA21	65	IOVDD	117	GND	169	CLK_CFG0
14	DATA20	66	ADDR6	118	VDD	170	BOOTCFG0
15	IOVDD	67	ADDR7	119	$\overline{\text{RD}}$	171	CLK_CFG1
16	GND	68	ADDR8	120	ACK	172	$\overline{\text{EMU}}$
17	DATA19	69	ADDR9	121	FLAG3	173	BOOTCFG1
18	DATA18	70	ADDR10	122	FLAG2	174	TDO
19	VDD	71	GND	123	FLAG1	175	DAI4
20	GND	72	VDD	124	FLAG0	176	DAI2
21	DATA17	73	GND	125	DAI20	177	DAI3
22	VDD	74	IOVDD	126	GND	178	DAI1
23	GND	75	ADDR11	127	VDD	179	IOVDD
24	VDD	76	ADDR12	128	GND	180	GND
25	GND	77	ADDR13	129	IOVDD	181	VDD
26	DATA16	78	GND	130	DAI19	182	GND
27	DATA15	79	VDD	131	DAI18	183	DPI14
28	DATA14	80	AVSS	132	DAI17	184	DPI13
29	DATA13	81	AVDD	133	DAI16	185	DPI12
30	DATA12	82	GND	134	DAI15	186	DPI11
31	IOVDD	83	CLKIN	135	DAI14	187	DPI10
32	GND	84	XTAL2	136	DAI13	188	DPI9
33	VDD	85	IOVDD	137	DAI12	189	DPI8
34	GND	86	GND	138	VDD	190	DPI7
35	DATA11	87	VDD	139	IOVDD	191	IOVDD
36	DATA10	88	ADDR14	140	GND	192	GND
37	DATA9	89	GND	141	VDD	193	VDD
38	DATA8	90	IOVDD	142	GND	194	GND
39	DATA7	91	ADDR15	143	DAI11	195	DPI6
40	DATA6	92	ADDR16	144	DAI10	196	DPI5
41	IOVDD	93	ADDR17	145	DAI8	197	DPI4
42	GND	94	ADDR18	146	DAI9	198	DPI3
43	VDD	95	GND	147	DAI6	199	DPI1
44	DATA4	96	IOVDD	148	DAI7	200	DPI2

Table 44. 208-Lead MQFP Pin Assignment (Numerically by Lead Number) (Continued)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
45	DATA5	97	ADDR19	149	DAI5	201	CLKOUT
46	DATA2	98	ADDR20	150	IOVDD	202	$\overline{\text{RESET}}$
47	DATA3	99	ADDR21	151	GND	203	IOVDD
48	DATA0	100	ADDR23	152	VDD	204	GND
49	DATA1	101	ADDR22	153	GND	205	DATA30
50	IOVDD	102	$\overline{\text{MS1}}$	154	VDD	206	DATA31
51	GND	103	$\overline{\text{MS0}}$	155	GND	207	DATA29
52	VDD	104	VDD	156	VDD	208	VDD

PACKAGE DIMENSIONS

The ADSP-21369 is available in a 208-lead, Pb-free MQFP package and 256-ball Pb-free and leaded SBGA packages

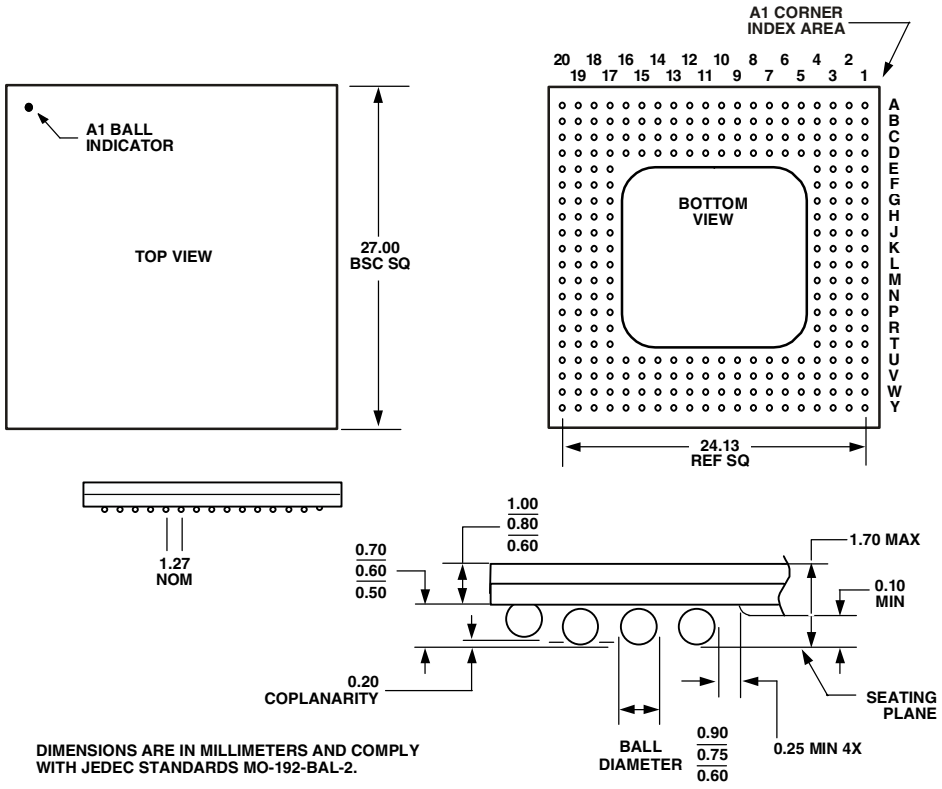
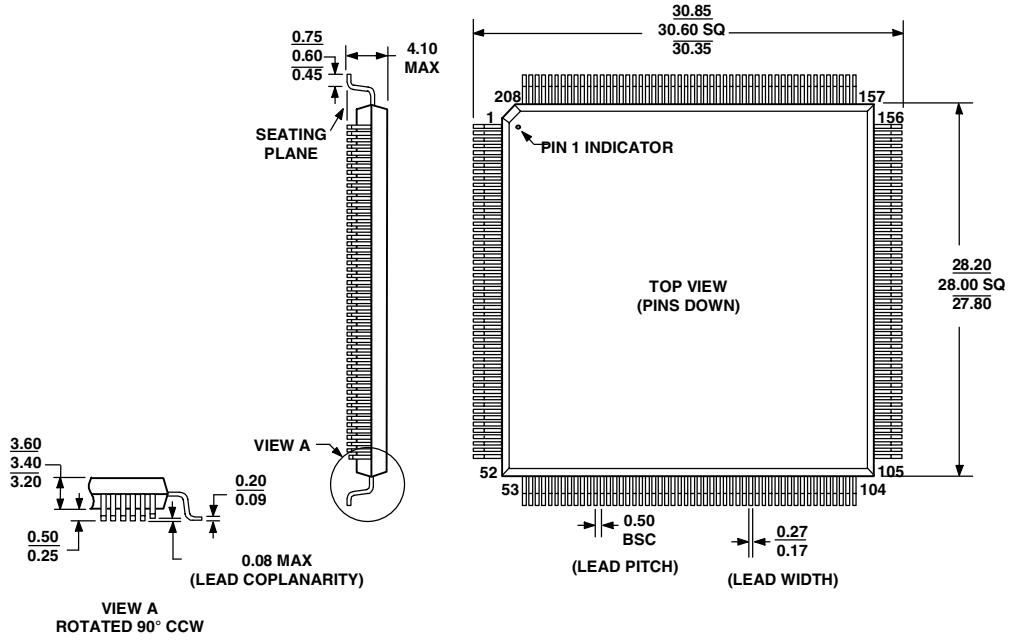


Figure 42. 256-Lead SBGA, Thermally Enhanced (BP-256)



NOTES:
1. THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION.
2. CENTER DIMENSIONS ARE TYPICAL UNLESS OTHERWISE NOTED.
3. DIMENSIONS ARE IN MILLIMETERS AND COMPLY WITH JEDEC STANDARD MS-029, FA-1.

Figure 43. 208-Lead MQFP (S-208-2)

ORDERING GUIDE

Part Number[1, 2]	Ambient Temperature Range	On-Chip SRAM	ROM (Reserved)[3]	Operating Voltage	Packages
ADSP-21369KSZ-ENG	0°C to +70°C	2M bit	6M bit	1.2 INT/3.3 EXT V	208-Lead MQFP, Pb-Free
ADSP-21369KBP-ENG	0°C to +70°C	2M bit	6M bit	1.2 INT/3.3 EXT V	256-Ball SBGA, Pb-Bearing
ADSP-21369KBPZ-ENG	0°C to +70°C	2M bit	6M bit	1.2 INT/3.3 EXT V	256-Ball SBGA, Pb-Free

[1] B indicates Ball Grid Array package.
[2] Z indicates Lead Free package. For more information about lead free package offerings, please visit www.analog.com.
[3] The ADSP-21369 processor includes a customer-definable ROM block. Please contact your Analog Devices sales representative for additional details.

PR05525-0-6/05(PrB)

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